ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

MSc THESIS

Erkan ERDEMLİ

A NEW APPROACH FOR N-STAGE RC LADDER NETWORKS BASED ON ELMORE DELAY MODEL

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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We certify that the thesis titled above was reviewed and approved for the award of degree of the Master of Science by the board of jury on __/__/2018.

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ABSTRACT

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Elmore delay model which is considered to be the most popular and unprecedented method of analog and digital integrated circuit delay calculations, is the main part of many design approaches ever since. Through delay calculations of VLSI circuits, distributed RC ladder networks are utilized as a modelling tool. Thus, delay calculation complexity of corresponding circuit is related with the stage number of RC ladder network. Thanks to Elmore delay model, complex calculations are easily done. In this thesis, a composed linear relation between SPICE simulation results, experimental test results and Elmore delay model is observed during researches for N-Stages RC ladder network. After characterizing the deviation problem between SPICE and Elmore delay, an improved Elmore delay model is proposed. The proposed delay model is extracted by applying Least Mean Square method on SPICE simulation results stated by experimental test results. The proposed method is tested on N-Stage RC ladders and test results are compared with that of SPICE simulation environment. All implementations of the proposed approach are done in MATLAB environment. Accordingly, the proposed method was shown to be significantly efficient.

Key Words: Elmore delay model, RC ladder networks, delay calculations, SPICE, MATLAB

ÖZ

YÜKSEK LİSANS TEZİ

ELMORE GECİKME MODELİNE DAYANILARAK N-KATMANLI RC MERDİVEN BAĞLANTILI DEVRELER İÇİN YENİ BİR YAKLAŞIM

Erkan ERDEMLİ

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Analog ve dijital entegre devre gecikme hesaplamalarında eşsiz ve yaygın olarak kullanılan Elmore gecikme modeli, günümüzde bir çok dizayn yaklaşımlarının ana parçası olmuştur. VLSI devrelerin gecikme hesaplamaları sayesinde dağınık RC merdiven ağlarından bir modelleme aracı gibi yararlanılmıştır. Böylece ilgili devrenin gecikme hesaplama karmaşıklığı RC merdiven ağının katman sayısı ile ilişkilendirilmiştir. Elmore gecikme modeli sayesinde de karışık hesaplamalar kolaylıkla yapılmıştır. Bu tez de N-Katmanlı RC merdiven ağı için SPICE simülasyon sonuçları, deneysel test sonuçları ve Elmore gecikme modeli arasında oluşan lineer ilişki, araştırmalar boyunca incelenmiştir. SPICE ve Elmore gecikme modeli arasında sapma problemi belirlendikten sonra Elmore gecikme modeline bir iyileştirme amaçlanmıştır. Amaçlanan gecikme modeli, deneysel test sonuçları ile belirlenmiş SPICE simülasyon sonuçları üzerine en az ortalama kareler metodunun uygulanması ile çıkarılmıştır. Önerilen metot N-Katmanlı RC merdiven ağlar üzerinde test edilmiştir ve test sonuçları SPICE simülasyon ortamının sonuçları ile karşılaştırılmıştır. Önerilen yaklaşımın bütün uygulamaları MATLAB'da yapılmıştır. Sonuç olarak önerilen metodun önemli ölçüde etkili olduğu gösterilmiştir.

Anahtar Kelimeler: Elmore gecikme modeli, RC merdiven bağlantıları, Gecikme hesaplamaları, SPICE, MATLAB

GENİŞLETİLMİŞ ÖZET

Dijital CMOS VLSI teknolojisinin hızlı gelişimi ile tasarlanmak istenen VLSI devreler büyümüş ve devrenin gecikme tahmin hesabını yapmak git gide karmaşıklaştığı ve zorlaştığı görülmüştür. Sadece devre tasarımında değil aynı zamanda MOS transistörlerinin üretimindeki güç tüketim hesabı, işlevsel özellikleri gibi birçok konuda gecikme tahminleri önemli rol oynadığı, VLSI devreleri tasarlayan tasarımcılar tarafından anlaşılmıştır. Bu nedenle VLSI literatürüne birçok gecikme tahmini yapabilen matematiksel yaklaşımlar girmiştir. Bunlardan biri de 1947 yılında W. ELMORE tarafından geliştirilen Elmore gecikme modelidir.

Elmore gecikme modeli lineer ağların gecikme hesabında diğer karmaşık matematiksel çözümlere göre daha basit bir yöntem geliştirmiş ve gecikme hesabındaki problemi çözmüştür. Böylece tasarımcılar VLSI devre tasarımlarında hızlı ve kolay çözümler üretebilmek için Elmore gecikme modelini RC merdiven, RC ağaç ve RLC devreler gibi farklı farklı devrelere göre uyarlayarak VLSI devrelerin gecikme tahmininde kullanmaya başlamıştır. Böylece Elmore gecikme modeli, VLSI tasarımlarındaki gecikme tahminleri yapmada VLSI tasarımcıları tarafından tercih sebebi olmuştur.

Gelişen VLSI tasarımlarıyla beraber Elmore gecikme modelin hesaplamadaki problemleri tespit edilmiş ve VLSI tasarımlarında daha iyi sonuçlar alabilmek için farklı matematiksel yaklaşımlar geliştirilmiştir. Böylece VLSI literatürüne Elmore gecikme modelinden daha doğru gecikme hesabı sonuçları verebilen hesaplama modelleri de girmiştir. Fakat bu modellerin Elmore gecikme modeline göre daha karmaşık yöntemlere sahip oldukları belirlenmiştir. Bu yüzden de Elmore gecikme modelin diğer hesaplama yaklaşımlara göre hızlı ve kolay bir metot olduğu kabullenilmiştir. Aynı zamanda Elmore gecikme modelinin hesaplamalardaki problemler üzerinde iyileştirmeler amaçlanarak, daha doğru gecikme hesabı yapabilmesi için birçok araştırma yapılmıştır.

Bu araştırmalardan birinde ise ilk önce Elmore gecikme modelinin gecikme hesaplamada ne gibi problemlerin olduğunu tespit edebilmek için N katmanlı RC merdiven devresi üzerinde durulmuştur. Ayrıca devre üzerindeki R (Direnç) 1kΩ ve C (Kapasitör) 1pF değerleri referans alınarak sabit parametreler oluşturulmuştur. Değişen katman sayısına göre N katmanlı RC merdiven devresinin gecikme hesaplamaları Elmore gecikme modeline göre hesaplanıp kayıt edilmiştir. Aynı zamanda N katmanlı RC merdiven devresinin transfer fonksiyon denklemi çıkartılarak MATLAB ortamında devrenin gecikme hesabı yapılmış ve devrenin SPICE ortamında da simülasyonları yapılarak alınan sonuçlar kayıt edilmiştir. Bununla beraber laboratuvar ortamında N katmanlı RC merdiven devresi kurularak osiloskop ölçüm aleti sayesinde alınan gecikme verileri de kayıt edilmiştir.

Kayıt edilen SPICE, MATLAB ve deney verilerinden referans datalar belirlemek için bu veriler MATLAB ortamında karşılaştırılmıştır. Sonuç olarak da SPICE simülasyon sonuç dataları daha kararlı olduğu ön görülmüş ve referans data olarak belirlenmiştir.

Referans data olarak belirlenen SPICE ile Elmore gecikme model sonuçları MATLAB ortamında karşılaştırılarak iki veri arasında ilişki kurulmuştur. Bununla beraber iki sonuç verileri arasında belli bir oranda sapma olduğu görülmüştür. Böylece sapma oranını belirlemek için Least Mean Square (En Küçük Kareler) matematiksel yöntemi kullanılarak iki data arasındaki sapma oranı belirlenmiştir. Belirlenen sapma oranı Elmore gecikme modeline eklenerek yeniden gecikme hesaplamalar yapılmış ve elde edilen yeni veriler SPICE sonuçlarıyla karşılaştırılarak yeni yaklaşımın doğruluğu test edilmiştir. Böylece VSLI literatürüne yeni bir Elmore gecikme modeli daha girmiştir.

Sonuç olarak, sapma problemi giderilen yeni Elmore gecikme modeli SPICE, MATLAB, deney sonuçları ve diğer gecikme modellerin gecikme sonuçları ile karşılaştırılarak başarı oranı belirlenmiştir. Elde edilen başarı oranlarına göre yeni Elmore gecikme modelinin başarılı olduğu görülmüştür.

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CONTENTS **PAGE**

ABSTRACT I
ÖZ II
GENİŞLETİLMİŞ ÖZET III
ACKNOWLEDGEMENTS V
CONTENTS VI
LIST OF TABLE VIII
LIST OF FIGURES X
1. INTRODUCTION 1
2. DELAY TIME CALCULATION METHODS 7
2.1. RC Time Constant 7
2.2. Step Response and Delay Time Calculation of RC Circuit 8
2.3. RC Ladder Circuit Network 11
2.4. Elmore Delay Model 15
2.5. Improved Elmore Delay Model 18
2.6. Modified Elmore Delay Model 19
2.7. Simulation and Experiment 19
2.7.1. SPICE Simulation 19
2.7.2. MATLAB Simulations 21
2.7.3. Experimental Results 23
3. NEW ELMORE DELAY MODEL 27
3.1. Definition of Reference Data 27
3.2. Definition of Problem 28
3.3. New Elmore Delay Model 29
4. CONCLUSION 39
REFERENCES 41
BIOGRAPHY 45

APPENDIX.....46

LIST OF TABLE **PAGE**

Table 3.1. List of K constant values.....36

LIST OF FIGURES **PAGE**

Figure 2.1. RC Charging Curves 8
Figure 2.2. RC Circuit 8
Figure 2.3. The capacitor discharging curves 11
Figure 2.4. N - Stage RC Ladder Network Model 12
Figure 2.5. 2 - Stage RC Ladder Circuit 12
Figure 2.6. 1-Stage RC Circuit 20
Figure 2.7. Simulation Result of 1-Stage RC Circuit 20
Figure 2.8. 2-Stage RC Circuit 20
Figure 2.9. Simulation Result of 2-Stage RC Circuit 20
Figure 2.10. Output Graph of 2 - Stage RC System 22
Figure 2.11. Experimental Result of 2-Stage RC Circuit 24
Figure 2.12. Experimental Result of 3-Stage RC Circuit 24
Figure 2.13. Experimental Result of 4-Stage RC Circuit 25
Figure 3.1. Graph of SPICE simulation and Experimental Results 27
Figure 3.2. Graph of SPICE simulation and MATLAB Results 28
Figure 3.3. Graph of SPICE simulation and Elmore Delay Calculation Results 29
Figure 3.4. Graph of SPICE simulation and New Elmore Delay Calculation Results 37

1. INTRODUCTION

Recently, delay estimation plays a very important role for design purposes in the field of digital CMOS VLSI technology. Accordingly, the aspect ratio decision of MOS transistors directly that affects manufacturing, power consumption, integration and functional operation of the integrated circuit, is considered crucial. In the case of dynamic integrated circuits, the delay is mainly utilized and considered an important factor (Shen, Cai, Hong, Hu and Lu, 2008; Avci and Yamacli, 2010). Only an effective delay approach can help a designer optimize aspect ratios. Therefore, a lot of delay calculation approaches are introduced in VLSI literature during the development of VLSI technology. The most popular and fundamental one of these delay calculation methods is known as the Elmore delay (Elmore, 1947). Hence, in VLSI terminology the more stage number means there is the more computational complexity (Landan, 1976; Roy 1977; Datta, Sahoo and Kar, 2010; Marinov and Shivakumar, 1996). Elmore delay with simple and fast calculation approach is still widely used by VLSI designers without any equivalent alternative (Ginneken, 1990; Morgenshtein, Friedman, Ginosar and Kolodny, 2008).

Elmore delay model in delay calculation of linear networks is illustrated more simply than other complex mathematical solutions for delay calculation problem and is used for calculation of low pass and multi-stage wide band amplifier (Elmore, 1947). After that, Elmore delay model was used in delay calculation of N-stage RC ladder circuits with closed form formulation (Landan, 1976; Roy, 1977). Moreover, in digital, analog and mixed electronic chips a delay occurs along with gate or functional block delays due to wire trees connecting transistors each other. Performance of corresponding integrated circuit is affected by wire length, size and interconnects. A proposed design of different connection models of digital circuits to reduce the length of wire and to change the topology of the circuit by using Elmore delay model is introduced by (Ginneken, 1990; Morgenshtein, Friedman, Ginosar and Kolodny, 2008). Even by the exception of circuit element and wire delays, the

placement process also causes a considerable amount of delay in VLSI. Elmore delay calculation has also been used to calculate certain delays (Pavlidis and Friedman, 2008). An approach to increase performance of integrated circuit by adding a load capacitance to the last stage of N-Stage RC ladder circuit is proposed by (Datta, Sahoo and Kar, 2010; Marinov and Shivakumar, 1996). In this work all delay calculations are also done by Elmore delay.

Elmore delay calculation is applied to delay calculation on different circuits as RC tree, RC ladder and RLC. Limits of Elmore delay model is sought in delay calculations. When Elmore delay calculation model is used for design automation as a performance metric, lower and upper bounds are described for understanding the accuracy and limitations for the corresponding application. Elmore delay measure has an absolute upper bound of a 50% delay of an RC tree response. A lower bound on the delay is also expressed by (Gupta, Tutuianu and Pileggi, 1997). Additionally, although Elmore delay is a simple and fast calculation method in delay calculation of RC tree and RC ladder networks, it is not easily adaptable for delay calculation of RLC circuits. Therefore, Elmore delay is modified for delay estimation of RLC circuits, furthermore delay calculation of RC tree networks and a simple calculation method is purposed as RLC delay calculating Elmore delay model by (Ismail, Friedman and Neves, 2000).

Although different delay calculation methods may have the ability to estimate more accurate than Elmore delay in some case studies, their calculation methods are complex and difficult to apply in all cases. Considerable two delay models are proposed for delay calculation of RC ladder networks to be alternative to Elmore delay with an acceptable easy calculation ability, namely, delay via two moments (D2M) and effective capacitance metric (ECM) approaches for RC tree circuit (Alpert, Devgan and Kashyap, 2001). Both metrics have properties of Elmore delay model in delay calculation and less error according to Elmore delay model. When two metrics are compared, D2M that has more accurate results is observed according to ECM, but the ECM method has an advantage over the other method in

which it is more favorable to optimization similar to the Elmore delay model. In Goel and Huang (1990)'s paper, a Different calculation method is developed from classical Elmore delay and introduced as a new method with Asymptotic Waveform Evaluation (AWE) name. It is applied to estimate delay of integrated circuits (Goel and Huang, 1990). AWE is also used to estimate delay of RC tree networks which is proposed in (Pillage and Rohrer, 1990). Unit step function input is applied to RLC tree network and delay is obtained by the simulation results. The results are compared with that of Elmore delay model and approximation problem of Elmore delay model is observed due to inductive effect on RLC tree networks. According to the previously mentioned research, by considering the deviation between simulation and Elmore delay analytic calculation, an analytical delay model based on first and second moments to incorporate inductance effects into the delay estimate for interconnection lines under step input is developed. Different mathematical models with better accuracy than Elmore delay model is investigated for RLC networks. Arbitrary threshold delays are estimated by an introduced two-pole based analytic model by (Kahng, Masuko and Muddu, 1997). Additionally, different methods from Elmore delay to calculate delay of digital gates and transistors due to resistive and capacitive effects in inner structure are also introduced. Due to simplicity, wide applicability of Elmore delay, the other delay calculation methods are not popularly used in MOS integrated circuit design. Some cases instead of calculating exact delay, delay estimation is described by the upper to the lower bound of output response of circuits (Rubinstein, Penfield and Horowitz, 1983).

In another work, delay calculation results of Elmore delay model are compared with gamma distribution calculation method calculation on RC tree networks. In another approach, delay of the circuit structure like RC tree is estimated with waveform evolution and curve fitting by using the (PDF) probability density function approaches (Lin, Acar and Pileggi, 1998). Even a newer approach is described with probability density function in fitting moment of impulse response

where the delay can be estimated from the probability table by (Kay and Pileggi, 1998).

There are a lot of alternative delay calculation models which are developed utilizing Elmore delay as a base. They are stated as modified or updated Elmore delay approaches for more accurate delay calculation results. In VLSI literature sometimes Elmore delay calculation results are fitted by using curve fitting techniques. More accurate delay calculations are purposed by these fittings. One of them is named as fitted Elmore delay model (Shen, Cai, Hong, Hu and Lu, 2008). In delay calculation of RC ladder with unit step input excitation, delay calculation problems of Elmore delay model is improved and deviation of classical Elmore delay model is reduced. When compared with simulation results of SPICE, improved Elmore delay model is seen better accurate than classical Elmore delay model (Avci and Yamacli, 2010). At the same time, in VLSI interconnect analysis, RC ladder circuit which is an applied input of a sinus wave form can be often encountered. Elmore delay model is used in delay calculation of these circuits as a modification model proposed by (Mal and Dhar, 2010).

In this thesis, the adversity of not using any delay calculation model to calculate the delay of RC Ladder circuit networks will be shown. Step input function will be applied in MATLAB program, furthermore, transfer functions obtained from the results of circuit analyses and delay of circuit will be calculated with MATLAB. Delay data values will be acquired from MATLAB calculation results. After that Elmore delay model will be illustrated and used for delay calculations of N-Stage RC ladder network circuits. Moreover, N-Stage RC ladder network circuit will be simulated with SPICE circuit simulation program, the obtained simulation data values are compared with experimental result data values of N-Stage RC ladder network circuit and accuracy of SPICE result data values will be provided approximately according to experimental results of N-Stage RC ladder network circuit. Deviation problem in delay calculation of Elmore delay model will be defined to compere SPICE simulation data values with Elmore delay calculation

values. In this thesis, a new proposed model to improve a solution for the Deviation problem for RC Ladder network circuits in delay calculation of Elmore delay model. The proposed delay model will be compared with Elmore delay model, experimental data results, MATLAB calculation results and SPICE simulation data results and success ratio of proposed delay model will be shown correspondingly.

In this part, some scientific researches which exist in VLSI literature is explained about RC ladder network, RC Tree network and RLC network. In chapter 2, some delays calculation models which exist in VLSI literature such as Elmore delay model, Improved Elmore delay, Modified Elmore delay and simulations of RC ladder circuit in SPICE and delay calculation with using a tool in MATLAB are described by examining. In chapter 3, Least Mean Square is explained and a new delay calculation model is developed based upon Elmore delay model for N-Stage RC ladder circuit. In chapter 4, all results of delay calculation model and SPICE simulation results are compared in MATLAB. Finally, conclusion and future work of this study are discussed.

2. DELAY TIME CALCULATION METHODS

As is known, frequency waves are applied in timing of circuits, such as square, saw tooth, trapezoidal, rectangular waves. Timing plays an important role in control of systems. Forms of these waves as amplitudes and continuous times are time dependent.

In this chapter, some of delay time calculation methods exists in VLSI literature are explained in detail such as step response plot of dynamic system code of MATLAB, Elmore Delay Model (Elmore, 1947), Improved Elmore Delay Model (Avci and Yamacli, 2010) and Modified Elmore Delay Model (Mal and Dhar, 2010).

2.1. RC Time Constant

As known, a capacitor is used to store energy and is a passive circuit component. Also the capacitor had been developed between two conductive layers to place a dielectric material. The capacitor that is used in electric circuits is an important circuit component.

A first order RC circuit is shown in the figure 2.2. If initial voltage value of capacitor (V_{C_0}) is assumed to be zero at t_0 time and when 5 V DC input voltage (V_{in}) is applied, a node of circuit, charging process of capacitor will happen. Since capacitors need a time limit for charging so, with applying voltage(V_{in}), the charging process of the capacitor cannot be completed at the same time. Therefore, the time that the capacitor needs for charging varies depending on the value of resistor and the capacitive effect of capacitor that is on charge regarding the current in the circuit. Moreover, the capacitor begins to charge up in regards to the time taken for the charge on the capacitor to reach 63% of its maximum possible voltage, in our curve $0.63(V_{in})$ is known as the **Time Constant (τ)** illustrated in figure 2.1. Mathematically it is represented as follows:

$$\tau = RC \tag{2.1}$$

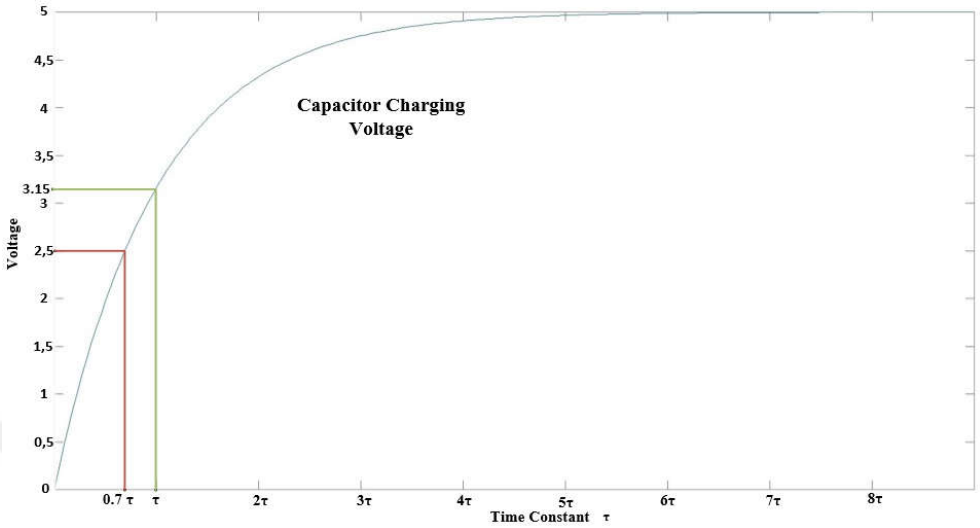


Figure 2.1. RC Charging Curves

2.2. Step Response and Delay Time Calculation of RC Circuit

The above mentioned RC circuit is illustrated in figure 2.2. When voltage (V_{in}) is applied; the current passing through a which is the node of circuit at $t_0 \geq 0$ time, will be at its maximum.

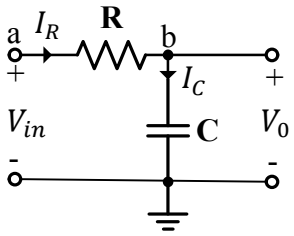


Figure 2.2. RC Circuit

After voltage is applied on the a node of circuit in $t_0 \geq 0$ time, the capacitor is charged by current that pass from the circuit as shown in the figure 2.1. Thus, the step respose function of RC circuit can be explained in terms of Kirchhoff's current law;

$$I_R = I_C \tag{2.2}$$

where I_R is represents the current that pass through the resistor of circuit. I_C is the current that pass through the capacitor of the circuit. Resistor (R) and capacitor (C) are serials on the circuit as shown in the figure 2.2. Because of that currents which pass through Resistor (R) and capacitor (C) are equal together as shown in Eq.2.2.

$$\frac{V_{in} - V_0}{R} = C\frac{dV_0(t)}{dt} \tag{2.3}$$

$$\frac{dV_0(t)}{V_0 - V_{in}} = -\frac{dt}{RC} \tag{2.4}$$

After that if the integral of equation 2.4 is taken according to $v(t)$ which represents the output voltage that is time dependent, and V_{C_0} which represents the initial voltage of the capacitor;

$$\ln(V_0 - V_{in})\Big|_{V_0}^{v(t)} = -\frac{t}{RC}\Big|_0^t \tag{2.5}$$

From Eq.2.5 we can conclude that:

$$\ln(v(t) - V_{in}) - \ln(V_{C_0} - V_{in}) = -\frac{t}{RC} + 0 \tag{2.6}$$

$$v(t) = V_{in} + \left(V_{C_0} - V_{in}\right)e^{\frac{-t}{RC}} \tag{2.7}$$

If the capacitor is initially uncharged, we set $V_{C_0} = 0$;

$$v(t) = V_{in}\left(1 - e^{\frac{-t}{\tau}}\right) \tag{2.8}$$

When a voltage with a voltage source 5 V DC input (V_{in}) of RC circuit is applied in figure 2.2, the capacitor will charge with the current passing through the circuit. After a certain time, the capacitor of the circuit will charge and if input voltage (V_{in}) of RC circuit is equaled zero, the capacitor behaves as open circuit. Charging time of capacitor will result in increasing the time done for that. Thus the capacitor will discharge. As a result, the output of the circuit will be plotted as illustrated in figure 2.3 according to Eq.2.7.

As shown in the figure 2.1 and the figure 2.3, the vertical red line is represented as a junction point of the charging and discharging timeline. Time delay of RC circuit from graph can easily be observed when analyzing the figure 2.1 and the figure 2.3. The junction point of charging and discharging voltage of the capacitor equals to the half of rise time and fall time of the voltage source. Time in this junction point is referred to the **Time Delay**. Thus time delay can be denoted in regards to Eq. 2.8;

$$v(t) = \frac{V_{in}}{2} \tag{2.9}$$

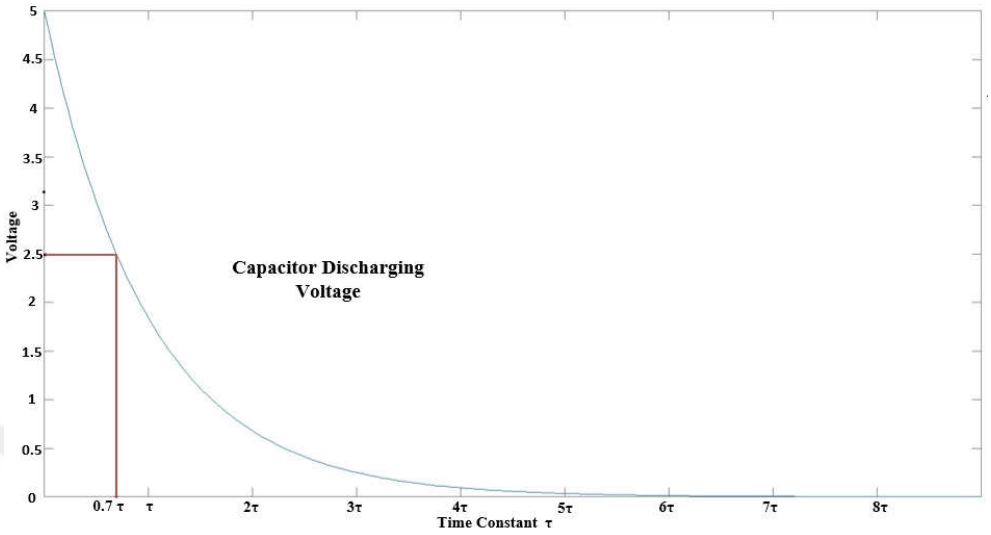


Figure 2.3. The capacitor discharging curves

$$\frac{V_{in}}{2} = V_{in}\left(1 - e^{\frac{-t}{\tau}}\right) \tag{2.10}$$

Taking the integral of Eq 2.10 the following equation is obtained,

$$\ln\left(\frac{1}{2}\right) = -\frac{t}{RC} \tag{2.11}$$

$$t = \ln(2)RC \tag{2.12}$$

where t represents the time delay.

2.3. RC Ladder Circuit Network

RC Ladder circuit network is happened to add until n resistance and n capacitance to one resistance and one capacitance to RC Circuit in the figure 2.2.

Every resistance and capacitance layer is called stage. Circuit as shown in the figure 2.4 is N – Stage RC Ladder circuit.

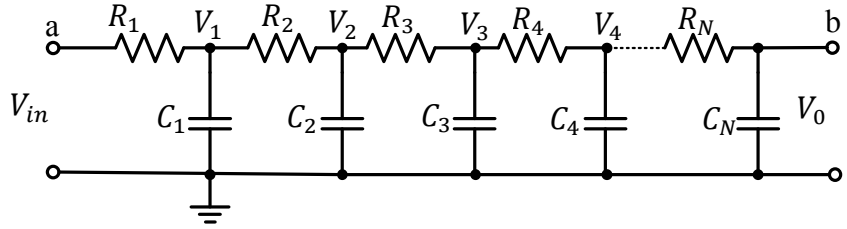


Figure 2.4. N - Stage RC Ladder Network Model

Transfer function of RC Ladder circuit can be explained with Kirchhoff's current law. Thus, delay of N-Stage RC ladder circuit can be calculated with algebraically methods.

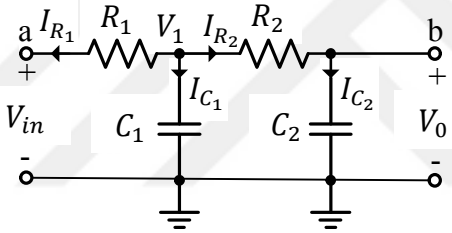


Figure 2.5. 2 - Stage RC Ladder Circuit

Transfer function of the 2 – Stage RC Ladder circuit can be obtained in the figure 2.5 by this way;

$$I_{R_1} + I_{C_1} + I_{R_2} = 0 \tag{2.13}$$

$$\frac{V_1 - V_{in}}{R_1} + \frac{V_1}{1/sC_1} + \frac{V_1 - V_0}{R_2} = 0 \tag{2.14}$$

$$\frac{V_0 - V_1}{R_2} + \frac{V_0}{1/sC_2} = 0 \tag{2.15}$$

Because of that

$$\frac{V_1 - V_{in}}{R_1} + \frac{2(V_1 - V_0)}{R_2} = V_0 sC_2 - V_1 sC_1 \tag{2.16}$$

$$\frac{V_1 - V_{in}}{R_1} = \frac{V_0 sC_2 R_2 - V_1 sC_1 R_2 - 2V_1 - 2V_0}{R_2} \tag{2.17}$$

$$V_{in} = \frac{V_0 sC_2 R_2 R_1 + V_1 sC_1 R_2 R_1 - 2V_1 R_1 - 2V_0 R_1}{R_2} - V_1 \tag{2.18}$$

In Fig 2.5, when the input voltage V_{in} is applied to the circuit of the stage RC Ladder, capacitors C_1 and C_2 start to charge while it reaches the voltage point V_1 passing through R_1. However, since the resistor R_2 is placed before capacitor C_2 it charges much slower than capacitor C_1 does. When capacitor C_1 is completely charged the input voltage V_{in} and voltage V_1 become equal in terms of value, accordingly, capacitor C_2 remains charging. As a result of that process, it is observed that the circuit mentioned above functions as the RC circuit. Furthermore, the input voltage V_{in} and voltage V_1 can be equal to one another, depending on the delay time that it takes to charge capacitor C_2 completely. As a result, by computing the equation of the input voltage V_{in} in terms of the first order of the RC, the equality to voltage V_1 can be determined and found as follows:

$$\frac{V_0 - V_{in}}{R_1} + \frac{V_0}{1/sC_1} = 0 \tag{2.19}$$

$$V_0 - V_{in} + V_0 s R_1 C_1 = 0 \tag{2.20}$$

$$V_{in} = V_0 (1 + s R_1 C_1) \tag{2.21}$$

$$V_{in} = V_1 \tag{2.22}$$

And

$$V_1 = V_{out} (1 + s R_1 C_1) \tag{2.23}$$

$$V_{in} = \frac{V_0 s C_2 R_2 R_1 + V_0 (1 + s R_1 C_1) s C_1 R_2 R_1 + 2 V_0 (1 + s R_1 C_1) R_1 - 2 V_0 R_1}{R_2} - V_0 (1 + s R_1 C_1) \tag{2.24}$$

If Eq.2.23 is simplified, the transfer function of 2 - Stage RC Ladder Circuit is

$$H(s) = \frac{1}{1 + s\left[R_1 C_1 + \left(R_1 + R_2 \right) C_2 \right] + s^2 R_1 C_1 R_2 C_2} \tag{2.25}$$

The function has two real poles and the step response is

$$V_0(t) = V_{in} . \frac{\tau_1 . e^{-t/\tau_1} - \tau_2 . e^{-t/\tau_2}}{\tau_1 - \tau_2} \tag{2.26}$$

with

$$\tau_{1,2} = \frac{R_1C_1 + (R_1 + R_2)C_2}{2} \cdot \left(1 \pm \sqrt{1 - \frac{\frac{4R_2C_2}{R_1C_1}}{\left[1 + \left(1 + \frac{R_2}{R_1}\right)\right]}} \right) \tag{2.27}$$

$$\tau_1 = R_1C_1 \tag{2.28}$$

$$\tau_2 = (R_1 + R_2)C_2 \tag{2.29}$$

If we accept $R_1 = R_2 = R$ and $C_1 = C_2 = C$

$$\tau = \tau_1 + \tau_2 = 3RC \tag{2.30}$$

Delay time of the circuit can be expressed with Eq.2.12

$$t = \ln(2)3RC \tag{2.31}$$

2.4. Elmore Delay Model

In 1947, Elmore delay calculation model that was developed by W.C. ELMORE was algebraically practical, easy, fast, and is not complex for delay calculation process according to other models (Elmore, 1947). At the same time, Elmore delay model is known as a general formula for calculating the propagation delay of a linear system given the transfer function of the linear system. If the transfer function of the linear system is $H(s)$, the normalized transfer function $h(s)$ is $H(s)/H(0)$, which can be generally expressed as

$$h(s) = \frac{1 + a_1 s + a_2 s^2 + ... + a_n s^n}{1 + b_1 s + b_2 s^2 + ... + b_m s^m} \tag{2.32}$$

where a_n and b_m are real and m>n. All the poles of $h(s)$ are real in a monotone response. At the same time, all the poles of $h(s)$ should lie on the negative real axis in a stable system. The unit step response of the normalized transfer function is $(1/s).h(s)$. The transient unit step response $h(t)$ is the first moment of the impulse response in the time domain. When the impulse response is taken as a probability distribution function (PDF), the mean can $h(t)$ be defined as the first moment of the impulse response. Thus, Elmore defined 50% of the delay time where $h(t)$ is equal to 0.5 as

$$T = \int_0^\infty th(t)dt \tag{2.33}$$

Thus, the transfer function $h(s)$ can be expressed in s domain as

$$h(s) = \int_0^\infty h(t)e^{-s.t}dt = 1 - s\int_0^\infty th(t)dt + \frac{s^2}{2!}\int_0^\infty t^2 h(t)dt - ... \tag{2.34}$$

$$h(s) = \sum_{i=1}^{\infty} \frac{1}{i!}(-s)^i \int_0^\infty h(t)t^i dt \tag{2.35}$$

If the transfer function of the system is set to increase its extent in s domain, Elmore delay time can be calculated and more accurate delay results can be obtained with this approximation.

Thus, in Elmore delay calculation method, time constant can be calculated by Eq. 2.35.

$$\tau = \sum_{i=1}^{N} R_{i,k} C_i \tag{2.36}$$

where N is the total number of nodes in the RC equivalent circuit, $R_{i,k}$ is the resistance of the portion of the path from C_i where C_i is the capacitance at node i. if Elmore delay model is used for delay calculation of N-Stage RC ladder circuit as shown in the figure 2.4, the derivation of the Elmore delay calculation model can be expressed as ;

$$R_1 = R_2 = ... = R_N = R_{eq} \tag{2.37}$$

$$C_1 = C_2 = ... = C_N = C_{eq} \tag{2.38}$$

If we assume that all resistors and capacitors of circuit equal to R_{eq} and C_{eq} respectively then we obtain:

$$\tau = R_{eq}C_{eq} + 2R_{eq}C_{eq} + 3R_{eq}C_{eq} + ... + NR_{eq}C_{eq} \tag{2.39}$$

where N is the total number of nodes in the RC equivalent circuit.

$$\tau = R_{eq}C_{eq}\sum_{i=1}^{N} n \tag{2.40}$$

$$\tau = R_{eq}C_{eq}\left(\frac{n(n+1)}{2}\right) \tag{2.41}$$

where τ is the time constant of N – Stage RC ladder network. Accordingly, we can calculate the delay by providing a step response as an input in Eq. 2.15 as follows:

$$0.5 = 1 - e^{-\frac{T_{Ed}}{R_{eq}C_{eq}\left(\frac{n(n+1)}{2}\right)}} \tag{2.42}$$

The result of Elmore delay calculation for N-Stage RC ladder circuit is shown below:

$$T_{Ed} = \ln(2) R_{eq} C_{eq} \left(\frac{n(n+1)}{2} \right) \tag{2.43}$$

2.5. Improved Elmore Delay Model

In a research held by Mutlu AVCI & Serhat YAMACLI a calculation model is proposed as a different approximation for Elmore delay model (Avci and Yamacli, 2010). Relying on this model, step response is applied to the circuit in figure 2.4. Deviations of data are illustrated between SPICE and Elmore delay model and a new general delay formula is extracted and observed. The new solution of the propagation delay referred to the improved Elmore model is derived according to the compound interest problem of Jacob Bernoulli.

$$T_{IEd} = \ln(2) R_{eq} C_{eq} \left(\frac{n + 0.884169384}{n \times 1.884169384} \right) \tag{2.44}$$

where T_{IEd} is the delay time according to the improved Elmore model. n is the stage number of RC Ladder network.

2.6. Modified Elmore Delay Model

Modified Elmore delay model which is developed by ASHIS KUMAR MAL & ANINDYA SUNDAR DHAR, describes a simple method of calculating a delay of an RC ladder by applying sinus wave form to the input of circuit shown in figure 2.4 (ASHIS KUMAR MAL, ANINDYA SUNDAR DHAR, 2010). In this model, R and C are identical and the transfer function in a closed form is derived as presented in figure 2.4. The roots of the transfer function are then observed in a closed form and the delay is calculated as shown in Eq.2.28 and Eq.2.29. A modified simple delay metric is proposed and used as a combination with the well-known Elmore delay method. As a result, and in regards to Elmore delay, the delay formula computed according to figure 2.4 is considered to be more accurate.

$$T_{MEd} \cong \frac{2.2R_{eq}C_{eq}}{\pi^2}\left[\frac{(2n+1)}{n}\right]^2 \tag{2.45}$$

where T_{MEd} is delay time according to the modified Elmore model. n is stage number of RC Ladder network.

2.7. Simulation and Experiment

2.7.1. SPICE Simulation

N-Stage RC circuit is simulated with 1 kΩ of R resistor value and 1 pF of C capacitor value to apply step response from 1 to 48 Stage using the SPICE simulation computer program. Moreover, when the voltage value of V_o reaches half of V_{in}, the delay data value of the circuit is obtained from the graphs extracted from the simulation process. Delay results are illustrated in table 1 of appendix.

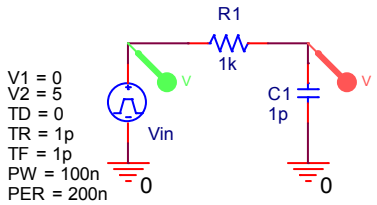


Figure 2.6. 1-Stage RC Circuit

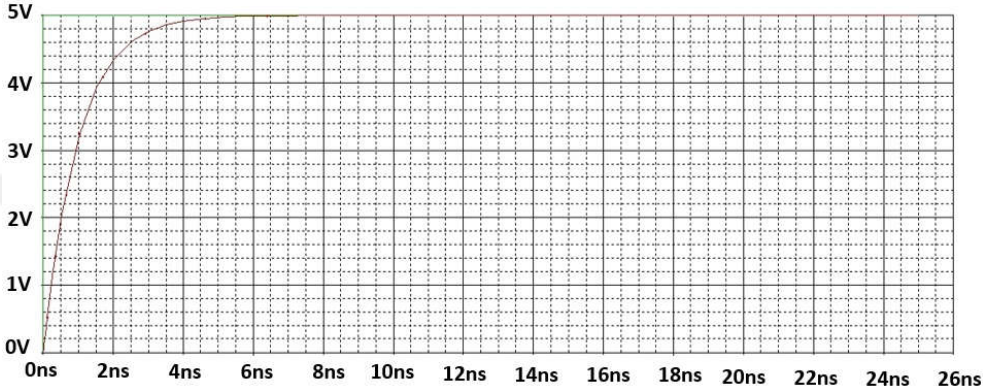


Figure 2.7. Simulation Result of 1-Stage RC Circuit

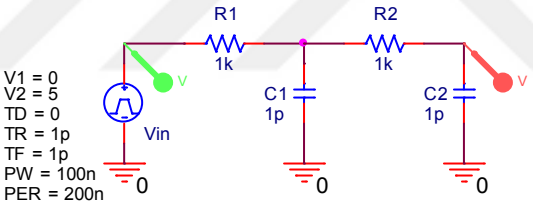


Figure 2.8. 2-Stage RC Circuit

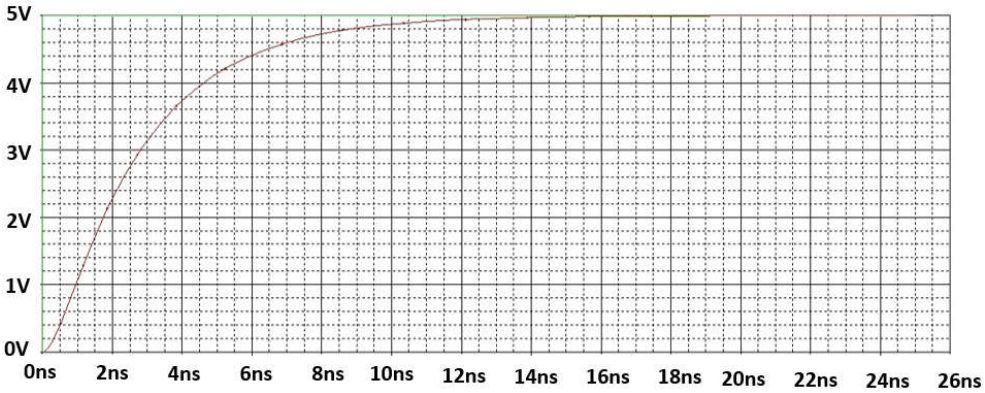


Figure 2.9. Simulation Result of 2-Stage RC Circuit

2.7.2. MATLAB Simulations

We can calculate the delay of N-Stage RC ladder using some known algebraic methods as Kirchhoff's Laws. But the delay calculation process will be complicated and difficult to compute especially, when the stage number of RC Ladder circuit increases. As a result, after the transfer function of the circuit is calculated with Kirchhoff's Laws method, transfer function graph of circuit can be extracted to use the step command in the MATLAB mathematical program. If delay is the time at which V_0 reaches $V_1/2$, delay can be observed from graph. Accordingly, it is assumed that the values of the resistors R_1, R_2 that are displayed in the circuit of the figure 2.5, are equal and their value is 1kΩ. Based on the same perspective, it is approved that capacitors C_1, C_2 are equal to a value of 1pF and therefore the transfer function is resolved as Eq.2.47 denotes:

$$H(s)=\frac{1}{R^2C^2s^2+3sRC+1} \tag{2.46}$$

$$H(s)=\frac{1}{10^{-18}s^2+3s10^{-9}+1} \tag{2.47}$$

Matlab code;

```
v2 = [10^(-18) 3 * 10^(-9) 1];
num = 5;
sys = tf(num, v2);
step(sys);
```

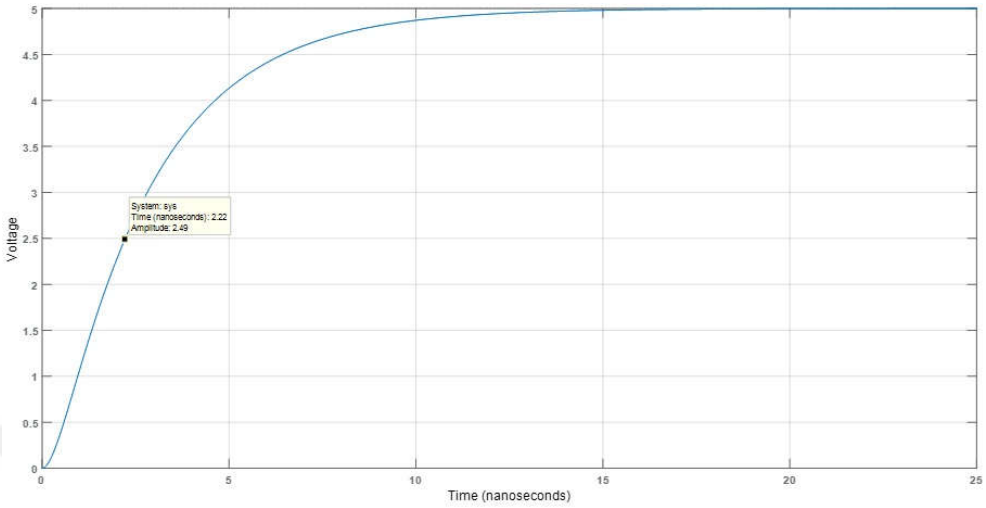


Figure 2.10. Output Graph of 2 - Stage RC System

Delay time of circuit from graph is illustrated in the figure 2.10. At the same time, delay of every stage of RC Ladder network can be by using the same command of MATLAB program. Moreover transfer functions of every stage of RC Ladder network can be calculated for delay calculation with MATLAB. However, for this process to function properly we need to consider using the mathematical equation of the transfer function that is presented in Eq.2.52.

$$V_1 = (1 + sRC)V_0 \tag{2.48}$$

$$V_2 = (2 + sRC)V_1 - V_0 \tag{2.49}$$

$$V_3 = (2 + sRC)V_2 - V_1 \tag{2.50}$$

$$V_4 = (2 + sRC)V_3 - V_2 \tag{2.51}$$

.

.

.

$$V_N = (2 + sRC)V_{N-1} - V_{N-2} \tag{2.52}$$

where $V_1, V_2, V_3, V_4, \ldots, V_N$ represents the V_{in} voltage of the 1-Stage, 2-Stage, 3-Stage and 4-Stage of the RC ladder circuit respectively. List of transfer functions that are shown from 1 stage until to 65 stage of RC Ladder circuit according to this method, are illustrated in table 2 of appendix.

Although delay of N-Stage RC Ladder circuit can be calculated by means of MATLAB, calculation of the transfer function will be slow in terms of time and will increase in terms of complexity and difficulty, when stage numbers of RC Ladder circuit increase. As a result, it is neither sufficient nor practical to compute the delay time of the N-Stage RC ladder circuit.

2.7.3. Experimental Results

N-Stage RC circuit is experimented using 1 kΩ of R resistor value and 1 pF of C capacitor value to apply step response ranging from 1 to 48 Stage. Moreover, when the voltage value of V_o reaches 2.5, the results of delay data value of the circuit is obtained from the graphs observed from computer interface program of the UNI-UT2000 oscilloscope model as shown in the figure 2.11, figure 2.12 and figure 2.13. Delay results are illustrated in table 1 of appendix.

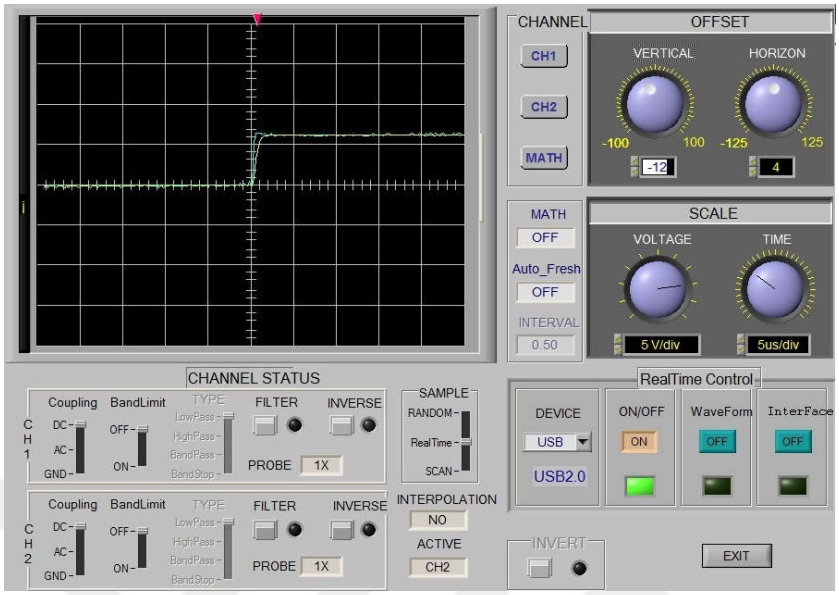


Figure 2.11. Experimental Result of 2-Stage RC Circuit

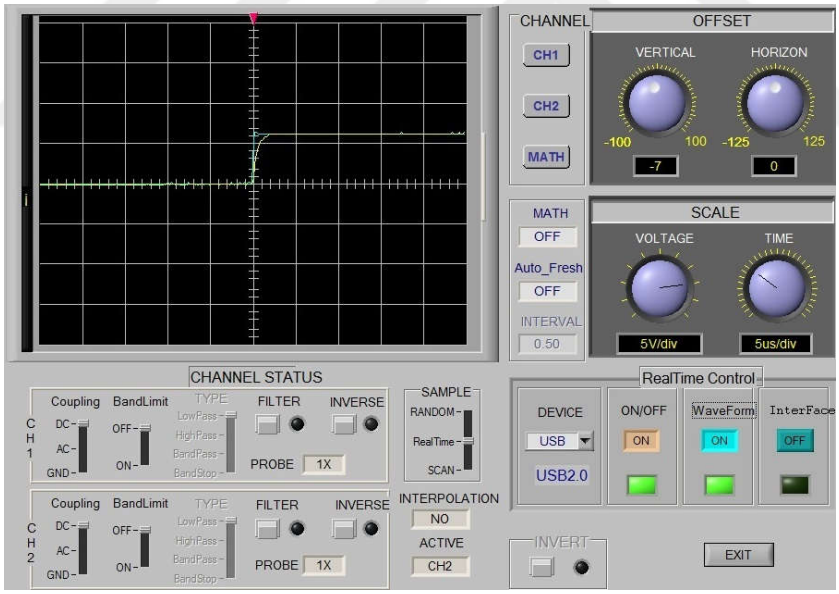


Figure 2.12. Experimental Result of 3-Stage RC Circuit

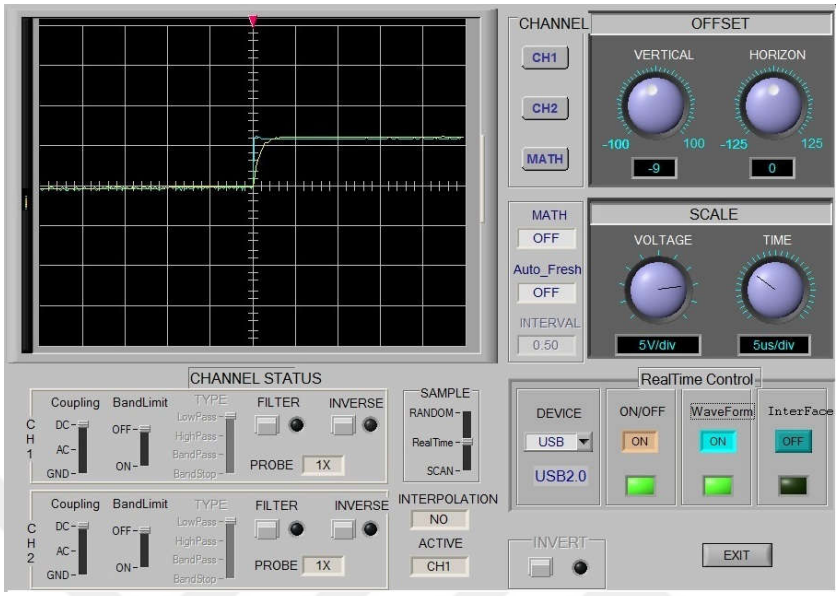


Figure 2.13. Experimental Result of 4-Stage RC Circuit

3. NEW ELMORE DELAY MODEL

In this chapter, firstly, we will define reference data and explain the problem of traditional Elmore delay calculation model about delay of N-Stage RC ladder network. After that, New Elmore delay model will be obtained to apply Least Mean Square to reference data with data of traditional Elmore delay.

3.1. Definition of Reference Data

In chapter 2, delay calculations have been explained with details and delay results data were denoted in table 1 of appendix. When observing the data in table 1 of appendix, experimental and MATLAB data values is compared with value of SPICE simulation on the graphs as shown in figure 3.1 and figure 3.2, additionally, it is clear that results of SPICE simulation is stable and the closest to which truth. Hence, MATLAB and Test results, SPICE simulation data can be accepted as reference data to apply Least Mean Square method.

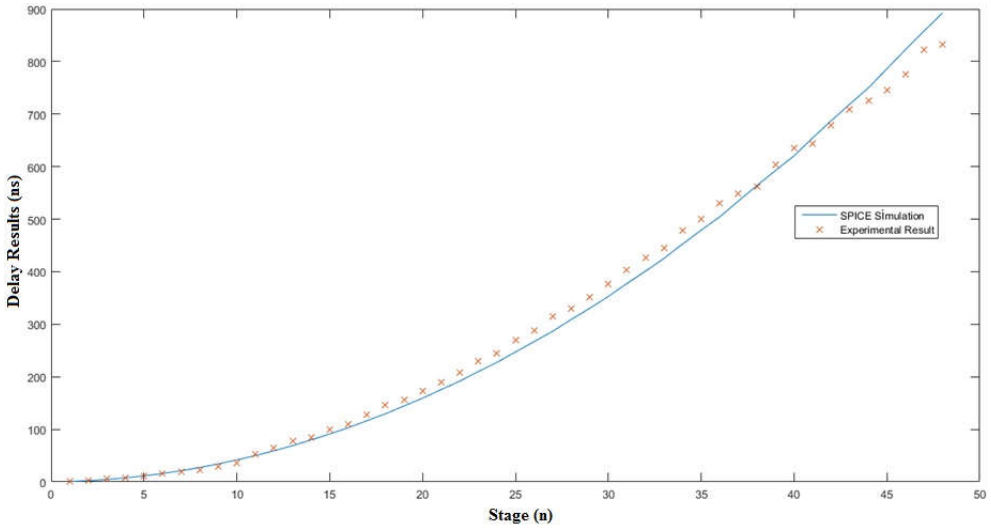


Figure 3.1. Graph of SPICE simulation and Experimental Results

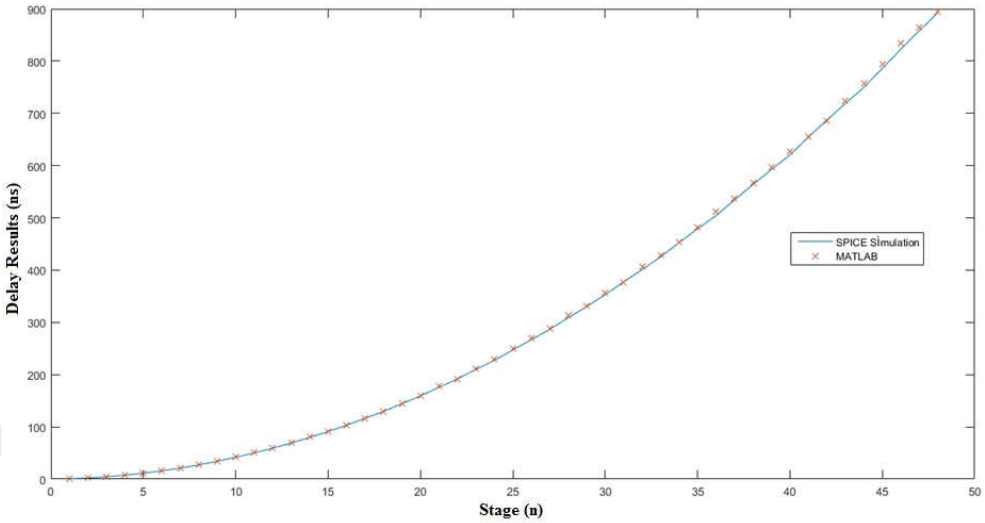


Figure 3.2. Graph of SPICE simulation and MATLAB Results

3.2. Definition of Problem

It is known that Elmore delay model has practical aspects for delay calculation in VLSI literature. Accordingly, Elmore delay model are still used by most of designers in integrating circuit design. Nevertheless, problems of Elmore delay model in delay calculation are investigated. When a linear relation between Elmore delay results and SPICE simulation results that had taken reference, is created, deviation of Elmore delay model is expressed on graph according to SPICE simulation results as shown in figure 3.3. Accuracy of Elmore delay model is discussed by VLSI integrating circuit designers.

Thus, in this thesis, reducing the deviation problem of Elmore delay model to use some mathematical method as Least Mean Square is proposed. Thanks to Least Mean Square mathematical method, Elmore delay model is improved, in delay calculation, we will obtain more accurate results from New Elmore delay model that will be developed.

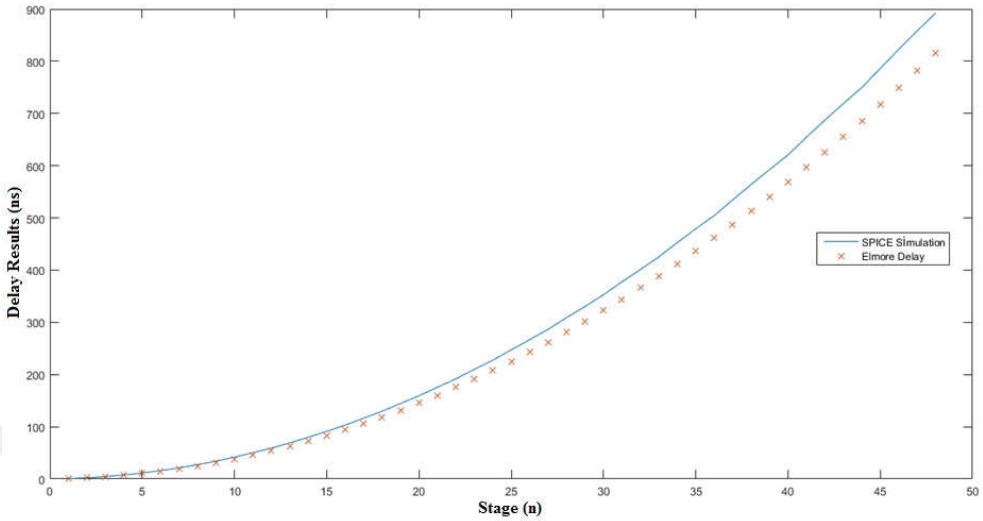


Figure 3.3. Graph of SPICE simulation and Elmore Delay Calculation Results

3.3. New Elmore Delay Model

Every time, linear relationships between experimental variables or the different mathematical theory calculation and simulation results should be found. Simulation and mathematical model results are obtained and tested accordingly. Thus if we assume that there is a linear relationship between simulation and mathematical calculation results as follows:

$$y = kx \tag{3.1}$$

where y is the force, x is the time, and k is the constant value. Therefore, we obtain data based on form (x_n, y_n) for $n \in \{1, \dots, N\}$; here y_n is the observed force when the time displaced x_n.

Moreover, it isn't possible to observe a perfect linear relationship for any system. Since two reasons exist. One of these is simulation error. The other is that the base calculation relationship may not be exactly linear according to the real system. Therefore, to determine what the "best fit" line is to the data, we use Least

Squares mathematical method. To quantify what we mean by "best fit", we will use some probability and statistics methods. If a sequence of data is $x_1, \dots, x_N$, we can define the mean to be $\frac{x_1+\cdots+x_N}{N}$. Therefore, this is referred by placing a line above x:

$$\bar{x} = \frac{1}{N}\sum_{n=1}^{N} x_n \tag{3.2}$$

The mean is the average value of the data. If the following two sequences of data is considered as $\{1,2,3,4,5\}$ and $\{3,3,3,3,3\}$, the same mean exist in both data sets. But there is greater variation for the first data set in terms of the mean. This pioneers the concept of variance, which is a useful tool to quantify how much a set of data undulates in regards to its mean. The variance of $\{x_1, \dots, x_N\}$, explained by σ_x^2, is

$$\sigma_X^2 = \frac{1}{N}\sum_{n=1}^{N}\left(x_i - \bar{x}\right)^2 \tag{3.3}$$

The square root of the variance equals to the standard deviation σ_x ;

$$\sigma_X = \sqrt{\frac{1}{N}\sum_{n=1}^{N}\left(x_i - \bar{x}\right)^2} \tag{3.4}$$

The x's and variance σ_x^2 represent the same units. Units of the standard deviation σ_x and the mean $\bar{x}$ represent the same units accordingly. Thus, we can calculate the standard deviation that gives a good measure of deviations of the x's in regards to their mean. At the same time, there are different measures that one can use. For example;

$$\frac{1}{N}.\sum_{n=1}^{N}\left(x_i - \bar{x} \right) \tag{3.5}$$

Unlikely, this is a signed quantity, and we can cancel from large positive to large negatives deviations. In fact, the definition of the mean illustrated above is zero. But when it is zero regardless of the values of the data, error represents the measurement of the variability in data. This problem can be rectified with using absolute values. Thus;

$$\frac{1}{N}\sum_{n=1}^{N}\left| x_i - \bar{x} \right| \tag{3.6}$$

Avoiding cancellation of errors results in an advantage, the absolute value function is not a good function according to analytic and differentiable. Hence, if $y = ax + b$, then $y - (ax + b)$ should be zero. Therefore;

$$\{(x_1, y_1),...,(x_N, y_N)\} \tag{3.7}$$

next

$$\{y_1 - (ax_1 + b),..., y_N - (ax_N + b)\} \tag{3.8}$$

The variance of this data set is

$$\sigma^2_{y-(ax+b)} = \frac{1}{N}\sum_{n=1}^{N}\left(y_n - (ax_n + b) \right)^2 \tag{3.9}$$

Due to taking the power in the equation, large errors give a higher weight according to smaller errors. Therefore we accept many medium sized errors over a few large errors. If absolute values are used to measure the error, all errors are weighted equally. As an alternative, if data are $\{(x_1, y_1), \dots, (x_N, y_N)\}$, we can define the error associated to saying $y = ax + b$ by;

SPICE and Elmore delay calculation result data are defined in table 1 of appendix . Moreover, the accuracy of SPICE simulation results is proved according to test and MATLAB calculation data. If Least Mean Square mathematical method is applied to the the obtained data from SPICE simulation and Elmore delay model , a deviation between SPICE and Elmore delay will be reduced as shown the figure 3.3. Thus, this linear relation can be stated as;

$$T_d = aT_e + b \tag{3.10}$$

where T_d is delay results is obtained from SPICE simulation. T_e denotes the results of Elmore delay calculation model. a and b are fitting constant values. Error analysis can be applied to find values of a and b with this equation.

$$E(a,b) = \frac{1}{N}\sum_{n=1}^{N}\left(T_{d_n} - \left(aT_{e_n} + b\right)\right)^2 \tag{3.11}$$

This represents N stage number and N times of the variance of the data set $\{T_{d_1} - (aT_{e_1}x_1 + b), \dots, T_{d_n} - (aT_{e_n} + b)\}$. Our aim is to find values of a and b that minimize the error. To find the values of (a, b) such that;

$$\frac{\partial E}{\partial a} = 0, \frac{\partial E}{\partial b} = 0 \tag{3.12}$$

If $E(a,b)$ yields is differentiated and then $\partial E/\partial a = \partial E/\partial b = 0$ is set and is divided by 2;

$$\frac{\partial E}{\partial a} = \sum_{n=1}^{N} 2\left(T_{d_n} - \left(aT_{e_n} + b\right)\right)\left(-T_{e_n}\right) \tag{3.13}$$

$$\frac{\partial E}{\partial b} = \sum_{n=1}^{N} 2\left(T_{d_n} - \left(aT_{e_n} + b\right)\right) \tag{3.14}$$

$$\sum_{n=1}^{N} 2\left(T_{d_n} - \left(a.T_{e_n} + b\right)\right)\left(-T_{e_n}\right) = 0 \tag{3.15}$$

$$\sum_{n=1}^{N} 2\left(T_{d_n} - \left(aT_{e_n} + b\right)\right) = 0 \tag{3.16}$$

We can rewrite these equations as

$$\left(\sum_{n=1}^{N} T_{e_n}{}^2\right)a + \left(\sum_{n=1}^{N} T_{e_n}\right)b = \sum_{n=1}^{N} T_{e_n} T_{d_n} \tag{3.17}$$

$$\left(\sum_{n=1}^{N} T_{e_n}\right)a + \left(\sum_{n=1}^{N} 1\right)b = \sum_{n=1}^{N} T_{d_n} \tag{3.18}$$

This approach can be used to calculate the values of a and b in which the error is minimized as shown below:

$$\begin{pmatrix} \sum_{n=1}^{N} 1 & \sum_{n=1}^{N} T_{e_n} \\ \sum_{n=1}^{N} T_{e_n} & \sum_{n=1}^{N} T_{e_n}{}^2 \end{pmatrix} \begin{pmatrix} b \\ a \end{pmatrix} = \begin{pmatrix} \sum_{n=1}^{N} T_{d_n} \\ \sum_{n=1}^{N} T_{e_n} T_{d_n} \end{pmatrix} \tag{3.19}$$

Since determinant of $\begin{vmatrix} N & \sum_{n=1}^{N} T_{e_n} \\ \sum_{n=1}^{N} T_{e_n} & \sum_{n=1}^{N} T_{e_n}{}^2 \end{vmatrix} \neq 0$. Cramer rule is applicable to obtain a and b variables;

$$a = \frac{\begin{vmatrix} \sum_{n=1}^{N} T_{d_n} & \sum_{n=1}^{N} T_{e_n} \\ \sum_{n=1}^{N} T_{d_n}.T_{e_n} & \sum_{n=1}^{N} T_{e_n}{}^2 \end{vmatrix}}{\begin{vmatrix} N & \sum_{n=1}^{N} T_{e_n} \\ \sum_{n=1}^{N} T_{e_n} & \sum_{n=1}^{N} T_{d_n}.T_{e_n} \end{vmatrix}} \tag{3.20}$$

$$b = \frac{\begin{vmatrix} N & \sum_{n=1}^{N} T_{d_n} \\ \sum_{n=1}^{N} T_{e_n} & \sum_{n=1}^{N} T_{d_n}.T_{e_n} \end{vmatrix}}{\begin{vmatrix} N & \sum_{n=1}^{N} T_{e_n} \\ \sum_{n=1}^{N} T_{e_n} & \sum_{n=1}^{N} T_{d_n}.T_{e_n} \end{vmatrix}} \tag{3.21}$$

According to data of SPICE and Elmore delay result that is obtained from table 1 of appendix in chapter 5, numerical results of Eq.3.20 and Eq.3.21 are $a =$

1.096 and $b = -6.662\ x10^{-11}$. As observed, b constant value is very close to zero. Therefore, b constant value may be neglected. A new fitting approach using equation 3.22 is shown below:

$$T_d = KT_e \tag{3.22}$$

where K is a rational constant between two time delays. Definition of error is illustrated in equation 3.23.

$$K = \frac{\sum_{n=1}^{N} T_{d_n} T_{e_n}}{\sum_{n=1}^{N} T_{e_n}^{\ 2}} \tag{3.23}$$

where T_d is the result of SPICE simulation and T_e is calculation result of Elmore delay.

$$T_{Ned} = K \frac{n(n+1)}{2} \ln(2) RC \tag{3.24}$$

$$T_{Ned} = \frac{\sum_{n=1}^{N} T_{d_n} T_{e_n}}{\sum_{n=1}^{N} T_{e_n}^{\ 2}} \frac{n(n+1)}{2} \ln(2) RC \tag{3.25}$$

where T_{Ned} is New Elmore delay model.

Table 3.1 List of K constant values

N-Stage(for R=1k-C=1p)	Spice	Elmore	K Constant Value	N-Stage(for R=1k-C=1p)	Spice	Elmore	K Constant Value
2	2.23172	2.07944	1.07323	**26**	266.76763	243.29466	1.09648
3	4.51555	4.15888	1.08576	**27**	286.61509	262.00963	1.09391
4	7.56055	6.93147	1.09076	**28**	308.99791	281.41776	1.09800
5	11.35249	10.39721	1.09188	**29**	330.28689	301.51902	1.09541
6	15.94413	14.55609	1.09536	**30**	352.92567	322.31344	1.09498
7	21.18669	19.40812	1.09164	**31**	377.50359	343.80100	1.09803
8	27.31431	24.95330	1.09462	**32**	401.00858	365.98171	1.09571
9	34.19856	31.19162	1.09640	**33**	425.36909	388.85557	1.09390
10	41.80689	38.12309	1.09663	**34**	452.79529	412.42257	1.09789
11	50.14729	45.74771	1.09617	**35**	479.02780	436.68272	1.09697
12	59.12987	54.06548	1.09367	**36**	504.48400	461.63602	1.09282
13	68.98244	63.07639	1.09363	**37**	534.32966	487.28247	1.09655
14	79.84478	72.78045	1.09706	**38**	563.97357	513.62206	1.09803
15	91.22856	83.17766	1.09679	**39**	592.59927	540.65480	1.09608
16	103.05690	94.26802	1.09323	**40**	620.56250	568.38069	1.09181
17	116.41308	106.05152	1.09770	**41**	654.62482	596.79972	1.09689
18	129.59691	118.52817	1.09338	**42**	687.28127	625.91190	1.09805
19	144.51320	131.69796	1.09731	**43**	718.91373	655.71723	1.09638
20	159.29965	145.56091	1.09438	**44**	749.83662	686.21571	1.09271
21	175.71802	160.11700	1.09744	**45**	786.24045	717.40733	1.09595
22	191.68517	175.36624	1.09306	**46**	822.73182	749.29210	1.09801
23	210.03795	191.30862	1.09790	**47**	858.06900	781.87002	1.09746
24	227.36282	207.94415	1.09338	**48**	892.56537	815.14108	1.09498
25	247.23062	225.27283	1.09747				

From Eq.3.23 when $n \to \infty$ the value of K constant has a mean of 1.098, which equals to $ln(3)$ approximately. A new formula is obtained as shown in Eq.3.27.

$$T_{Ned} = \ln(3)\frac{n(n+1)}{2}\ln(2)RC \tag{3.26}$$

$$T_{Ned} = 0,7615000104\frac{n(n+1)}{2}RC \tag{3.27}$$

where T_{Ned} is the New Elmore delay result. n is the stage number. R and C are resistor and capacitor values. Delay of RC ladder circuits can be calculated fast, easy and more accurate compared to traditional Elmore delay calculation method by the formula obtained in Eq.3.27.

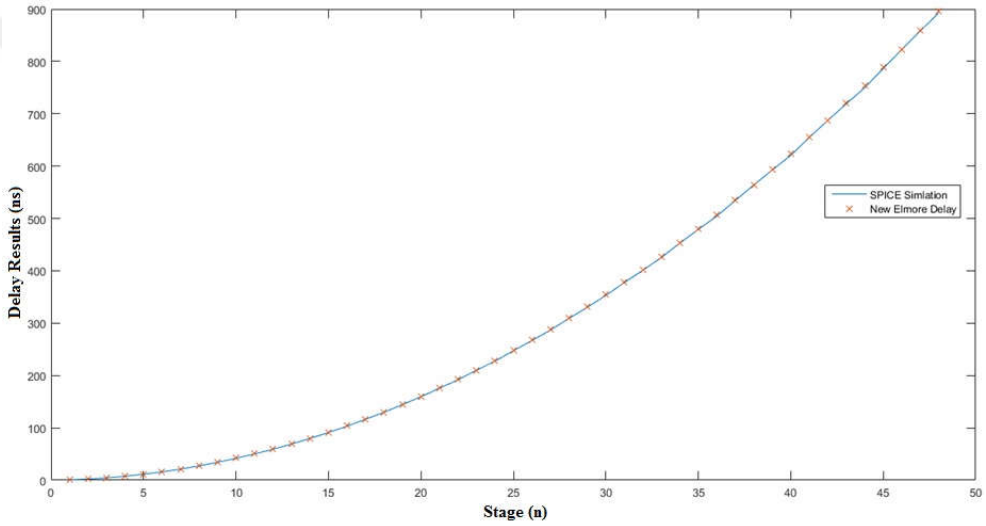


Figure 3.4. Graph of SPICE simulation and New Elmore Delay Calculation Results

4. CONCLUSION

In this study, when delay calculations of RC ladder networks are expressed by Kirchhoff's current law and at the same time, stage number of RC ladder networks are increased, the complexity and difficultly of calculations in the delay calculations are illustrated. Thanks to Elmore delay model, complex calculations are easily done. Moreover, transfer function algorithm of N-Stage RC ladder circuit have been denoted in the s domain using a well-known mathematical method which is Kirchhoff's Laws for discovering and observing the reason that falls behind the problem occurring in the delay calculation step. The step tool in MATLAB program was used to generate the delay calculation results of RC ladder circuit and accordingly illustrated in table 1 of appendix. Additionally, to SPICE simulation, experimental, Elmore delay, Modified Elmore delay and Improved Elmore delay calculation results of RC ladder circuit have been illustrated in table 1 of appendix.

At the same time, SPICE simulation result data with MATLAB mathematical computer program and experimental results have been compared to illustrate reference data set and to provide accuracy of SPICE simulation results according to MATLAB and experimental results. It has been seen that comparison of the results yielded an ideal and acceptable data with regards to SPICE simulation results.

After that linear relation has been identified and observed between SPICE and Elmore delay. It has been seen that a deviation in Elmore delay results according to SPICE exists. From this linear relation, the reason caused behind the problem presented in delay calculation has been illustrated and discussed. Thus, in order to reduce the deviation of Elmore delay model results, Least Mean Square mathematical method has been used and a new formula was proposed accordingly.

Consequently, results of all calculation models have been listed in table 5.1. Furthermore, the success rate of delay models has been significantly shown in the thesis. According to reference data set SPICE simulation, the average success rate is

% 99.38 for MATLAB, % 98.52 for the Experimental results, % 91.25 for the Elmore delay, % 96.52 for the Improved Elmore delay, % 34.88 for the Modified Elmore delay and % 99.75 for the New Elmore delay, which yielded an improvement regarding this study case. As shown in average success rate of the New Elmore Delay formulation, the New Elmore delay for delay calculation of RC ladder network is obtained and yielded more accurate results according to average success rate of other delay models. The New Elmore delay formulation can be easily integrated into the design automation tools without any increment in the computational cost. Which means it is a practical method to use in real life applications.

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BIOGRAPHY

Erkan ERDEMLI was born in Sivas on May 6, 1984. He graduated from Mersin Yıldırımhan Anatolian High School in 2002 and entered to Electrical & Electronics Engineering Department of Fatih University in 2002 and graduated in 2007. He has been working in Alperen Engineering Company as manager since January 2008.

APPENDIX