ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES

MSc THESIS

Yeliz YOLDAŞ

DESIGN AND SIMULATION OF DSTATCOM FOR POWER QUALITY IMPROVEMENTS

DEPARTMENT OF ELECTRICAL AND ELECTRONICS ENGINEERING

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We certify that the thesis titled above was reviewed and approved for the award of degree of the Master of Science by the board of jury on 18/02/2015.

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ABSTRACT

MSc THESIS

DESIGN AND SIMULATION OF DSTATCOM FOR POWER QUALITY IMPROVEMENTS

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ÇUKUROVA UNIVERSITY
INSTITUTE OF NATURAL AND APPLIED SCIENCES
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The increased perception in power quality topics has provided important changes and improvements in power electronics devices. This devices are used to maintain and improve the power quality and reliability of distribution system and to protect customers/users against disturbances generated by other users in the network. Distribution Static Compensator (DSTATCOM) is a shunt connected power electronic device that can quickly mitigate power quality disturbances in the system.

The proposed DSTATCOM is connected in shunt to 400 V test system. Simulations have been performed to illustrate the effectiveness of the DSTATCOM. The results obtained from the simulations clearly showed that the designed DSTATCOM simultaneously performs the reactive power compensation, voltage regulation, harmonic elimination, load balancing, balanced voltage sag/swell and unbalanced voltage sag mitigation. Furthermore, by connecting a delta connected inductor-capacitor-inductor (LCL) passive filter at inverter output, the high order harmonics generated by the DSTATCOM can be easily and effectively eliminated.

In this thesis, a proposed DSTATCOM that protects a 300-kVA sensitive load is analyzed, modeled and simulated. The performance and efficiency of the proposed system are tested with different simulation cases by PSCAD/EMTDC program.

Key Words: Distribution Static Compensator, Voltage Sag/Swell, Harmonic Elimination, Power Factor Correction, Voltage Regulation

ÖZ

YÜKSEK LİSANS TEZİ

GÜÇ KALİTESİNİN İYİLEŞTİRİLMESİ İÇİN DSTATKOM'UN TASARIMI VE SİMÜLASYONU

Yeliz YOLDAŞ

ÇUKUROVA ÜNİVERSİTESİ
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Güç kalitesi konusundaki artan bilinç, güç elektroniği cihazlarında önemli iyileşmeler ve değişimler sağlamıştır. Bu cihazlar şebekede diğer kullanıcılar tarafından üretilen bozukluklara karşı müşterileri/kullanıcıları korumak, dağıtım sisteminin güvenilirliliğini ve güç kalitesini iyileştirmek ve korumak için kullanılır. Dağıtım Sistemi Statik Senkron Kompanzatörü (DSSSK) sistemdeki güç kalitesi bozukluklarını hızlı bir şekilde azaltabilen paralel bağlı bir güç elektroniği cihazıdır.

Önerilen DSSSK 400V test sistemine paralel bağlıdır. Simülasyonlar DSSSK'nın etkisini göstermek için gerçekleştirilmiştir. Simülasyonlardan elde edilen sonuçlar, tasarlanan DSSSK'nın eş zamanlı olarak reaktif güç kompanzasyonu, gerilim regülasyonu, harmonik eleme, dengeli gerilim düşümü/yükselmesi ve dengesiz gerilim düşümü düzeltimi yaptığını açıkça göstermektedir. Ayrıca, doğrultucu çıkışına üçgen bağlı bobin-kondansatör-bobin (BKB) pasif filtresi bağlayarak, DSSSK tarafından üretilen yüksek dereceli harmonikler kolayca ve etkin bir şekilde yok etmektedir.

Bu tez çalışmasında, 300-kVA'lık bir hassas yükü koruyan DSSSK'nın analizi, modellemesi ve simülasyonu yapılmıştır. Önerilen sistemin performansı ve verimliliği PSCAD/EMTDC programında farklı simülasyon çalışmalarıyla incelenmiştir.

Anahtar Kelimeler: Dağıtım Sistemi Statik Senkron Kompanzatörü, Gerilim Düşümü/Yükselmesi, Harmonik Eleme, Güç Faktörü Düzeltimi, Gerilim Regülasyonu

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LIST OF SYMBOLS

B_l : Load Susceptance

C_{DC} : DC Link Capacitor

C_f : Filter Capacitance

dB : Desibel

f_n : Nominal Frequency

f_{res} : Resonance Frequency

f_{sw} : Switching Frequency

G_l : Load Conductance

I_{THD} : Total Harmonic Distortion of Current

IHD_V : Voltage Individual Harmonic Distortion

IHD_I : Current Individual Harmonic Distortion

If : Rated RMS Current of Fundamental

I_h : Rated RMS Current of Each Harmonic

I_L : Rated RMS Value of Maximum Demand Load Current

I_{sc} : Maximum Short Circuit Current at PCC

I_S : Source Current

$I_{capacitive}$: Capacitive Current of DSTATCOM

$I_{inductive}$: Inductive Current of DSTATCOM

I_R : Resistive Component of Load Current

I_X : In-phase Component of Load Current

$I\gamma$: Compensator Current

I^0 : Zero Sequence of Current

I^- : Negative Sequence of Current

I^+ : Positive Sequence of Current

L_d : Choke Inductance

L_{dc} : DC Inductance

I_{load} : Load Current

L_f : Filter Inductance

L_g : Grid Side Inductance

L_i : Inverter Side Inductance

L_{DC} : DC Link Inductor

m_a : Modulation Index

P : Active Power

Q : Reactive Power

$Q_{capacitive}$: Capacitive Reactive Power of DSTATCOM

$Q_{inductive}$: Inductive Reactive Power of DSTATCOM

R_d : Damping Resistor

S : Apparent Power

S_l : Load apparent power

T : Time Period

w : Fundamental Frequency (rad/s)

w_{sw} : Switching Frequency (rad/s)

V_{DC} : DC Link Voltage

$Vpcc$: PCC Voltage

$V_{coupling}$: Voltage Drop Caused by Coupling Impedance

V_{dcref} : Reference DC Voltage

Vf : Rated RMS Voltage of Fundamental

V_h : Rated RMS Voltage of Each Harmonic

V_I : Inverter Output Voltage

V_{LL} : Line to Line Voltage

V_m : Peak Value of Voltage

V_{PCC} : Voltage of Point Of Common Coupling

V_{ref} : Reference Voltage at PCC

V_s : Source Voltage

V_{sag} : Voltage Magnitude at PCC during Sag

V_{THD} : Total Harmonic Distortion of Voltage

V^0 : Zero Sequence of Voltage

V^- : Negative Sequence of Voltage

V^+ : Positive Sequence of Voltage

Y_l : Load Admittance

Z_F : Fault Impedance

Z_s : Source Impedance

LIST OF ABBREVIATIONS

AC	: Alternating Current
ASD	: Adjustable Speed Drive
ADALINE	: Adaptive Linear Neuron
BP	: Back Propagation Based Theory
CSI	: Current Source Inverter
DSTATCOM	: Distribution Static Compensator
DVR	: Dynamic Voltage Restorer
DSP	: Digital Signal Processor
FFT	: Fast Fourier Transform
FPGA	: Field Programmable Gate Array
GTO	: Gate Turn-Off Thyristor
DC	: Direct Current
IEC	: International Electrotechnical Commission
IEEE	: Institute of Electrical and Electronics Engineers
et al.	: And Others
IGBT	: Insulated Gate Bipolar Thyristor
IHD	: Individual Harmonic Distortion
ISCT	: Instantaneous Symmetrical Component Theory
LMS	: Least Mean Square
MMF	: Motor Magnetic Field
NN	: Neural Network
PCC	: Point of Common Coupling
PI	: Proportional-Integral
PLL	: Phase Locked Loop
PQ	: Power Quality
p.f.	: Power Factor
PWM	: Pulse Width Modulation
RDFT	: Recursive Discrete Fourier Transform
RMS	: Root Mean Square

SLGF	: Single-Line to Ground Fault
SMES	: Superconducting Magnetic Energy Storage
SPWM	: Sinusoidal PWM
SRF	: Synchronous Reference Frame
SSC	: Static Series Compensator
SVB	: Series Voltage Booster
SVM	: Space Vector PWM
TDD	: Total Demand Distortion
THD	: Total Harmonic Distortion
UPQC	: Unified Power Quality Conditioner
UPS	: Uninterruptible Power Supply
VFD	: Variable Frequency Motor Drives
VSI	: Voltage Source Inverter

1. INTRODUCTION

1.1. Background and Research Motivation

Power quality is defined as the concept of powering and grounding electronic equipment in a manner that is suitable to the operation of that equipment and compatible with the premise wiring system and other connected equipment in Institute of Electrical and Electronics Engineers (IEEE) Standard 1159-1995 (IEEE Std 519, 1995).

Power quality is a topic in the area of engineering that emerged in the 1970s. It is a field that has attracted special interest recently due to the rapid growth in the industrial, raise of power demands with a growing population and the proliferation of "polluting" electrical loads. One of the objectives of power quality is to meet a form of clean sinusoidal, stable, reliable, regulated and uninterrupted supply voltage in electrical systems, in order to feed the so-called critical loads. A critical load is equipment that, if it works inadequately, it can cause very high losses; and a low quality supply can cause this situation. For example, it can cause the loss of vital information, interruption of an expensive industrial process, poor quality or damage to products; interruption of important communications as air traffic control, security units and financial information; permanent damage to equipment and even put lives in danger at hospitals. The great increment in critical processes has led to the requirement of assuring a high quality and safe power supply in many medical, communications and industrial procedures, with the aim of feeding machinery and automatic systems that perform diverse important tasks (González and Cárdenas, 2010). Thus in this changed scenario in which the customers increasingly demand quality power, the term *power quality (PQ)* attains increased significance (Ghosh and Ledwich, 2002).

Power quality problems in industrial applications concern a wide range of disturbances, such as voltage sags and swells, flicker, interruptions, harmonic distortions etc. To solve these problems, several different *Custom Power* devices have been proposed. The term *Custom Power* has been defined as "the concept of

employing power electronic (static) controllers in 1kV through 38kV distribution systems for the purpose of supplying a compatible level of power quality necessary for adequate performance of selected facilities and processes" (Cilona, 2010).

Distribution Static Compensator (DSTATCOM) is one of the custom power devices, a shunt compensation device which is generally used to solve power quality problems in distribution systems. The main advantage of DSTATCOM is that, it has a very sophisticated power electronics based control which can efficiently regulate the current injection into the distribution bus. The second advantage is that, it has multifarious applications, e.g. canceling the effect of poor load power factor, suppressing the effect of harmonic content in load currents, regulating the voltage of distribution bus against sag/swell etc, compensating the reactive power requirement of the load and many more (Sumner et al., 2006).

1.2. Aim and Outline of This Thesis

The aim of this thesis is to improve, analyze and test, via simulation, control algorithms for shunt-connected VSC, for reactive power compensation, voltage regulation, harmonic elimination, load balancing, balanced voltage sag/swell and unbalanced voltage sag mitigation.

After an introductory section where the background, research motivation and contribution of the study are introduced, the structure of this thesis is as follows:

In Chapter 2, defines the custom power term and some definitions related to the power quality issue used along the thesis. The causes and characteristics properties of the power quality problems are analyzed and the mitigation techniques of problems are discussed.

In Chapter 3, overview and wide literature survey of DSTATCOM are explained in detail. The circuit configuration, operation and basic functions are presented.

In Chapter 4, the power system parameters of DSTATCOM components are designed in PSCAD/EMTDC program for simulation cases. The equations derived in other chapters are adopted for the design of DSTATCOM components.

In Chapter 5, different case studies are performed to validate the performance of proposed control strategy and to verify the behavior of modeled DSTATCOM under various dynamic conditions.

In Chapter 6, the important conclusions of the study are explained and the future work topics on DSTATCOM are presented.

1.3. Contributions of Thesis

The main differences and important contributions of this thesis can be summarized as follows:

(i) DSTATCOM is a relatively popular device and not much work has yet been reported on its theoretical, design procedure and analysis. The publications made as a result of this thesis will contribute to scientific literature. This thesis will contribute to the concept finding solutions to the simultaneous mitigation of electric power quality problems such as load unbalance, harmonic, balanced voltage sag/swell, unbalanced voltage sag and reactive power compensation.

(ii) DSTATCOM control algorithm is optimized for simultaneous mitigation of electric power quality problems. The disadvantage of traditional control algorithms to calculate reference signal under unbalanced faults is eliminated.

(iii) The wide literature survey for DSTATCOM topologies and control algorithms has been accomplished.

(iv) To overcome the disadvantageous of traditional passive filters, a delta connected LCL filter that is newly developed configuration is designed and adopted for DSTATCOM application.

2. POWER QUALITY TERMS AND MITIGATION

Power quality is an issue that is becoming increasingly important to electricity consumers at all levels of usage. Sensitive equipment and non-linear loads are now more commonplace in both the industrial commercial sectors and the domestic environment. Because of this a heightened awareness of power quality is developing amongst electricity users. Occurrences affecting the electricity supply that were once considered acceptable by electricity companies and users are now often considered a problem to the users of everyday equipment (Stones and Collinson, 2001).

There are three major reasons for the increased concern on power quality (Dugan et al., 2004):

- Newer-generation load equipment, with microprocessor-based controls and power electronic devices, is more sensitive to power quality variations than was equipment used in the past.
- The increasing emphasis on overall power system efficiency has resulted in continued growth in the application of devices such high-efficiency, adjustable-speed motor drives and shunt capacitors for power factor correction to reduces losses. This is resulting in increasing harmonic levels on power systems and has many people concerned about the future impact on system capabilities.
- End-users have an increased awareness of power quality issues. Utility customers are becoming better informed about such issues as interruptions, dips, harmonics and switching transients and are challenging the utilities to improve the quality of power delivered.

2.1. Characterization of Electric Power Quality

The term electric power quality broadly refers to maintaining a near sinusoidal power distribution bus voltage at rated magnitude and frequency. In

addition, the energy supplied to a customers must be uninterrupted from the reliability point of view (Kusko and Thompson, 2007; Sarıbulut, 2012).

Most PQ problems occur in distribution systems. In most metropolitan cities, the distribution feeders run underground in the central business districts. In most other places the feeders run overhead. As a result these lines can easily come in contact with trees. Furthermore, they are likely to be hit by lightning or suffer from interference from birds and smaller animals. Moreover distribution systems feed loads directly. It is at these low voltage connections that the power quality becomes significantly worse. The utility has very little control over the loads. Furthermore, switching on of a large induction motor can cause a large inrush current to flow in that circuit causing a voltage dip in other parts of the system. In addition, some of the loads may have poor power factors causing unnecessary power loss in the distribution feeders.

Based on the above discussions, we can summarize that there are two different categories of causes for the deterioration in power quality (Ghosh and Ledwich, 2002). The first category contains natural causes such as:

- Faults or lighting strikes on transmission lines or distribution feeders.
- Falling of trees or branches on distribution feeders during stormy conditions.
- Equipment failure.

The second category contains the man made causes that may be due to load or feeder/transmission line operation. Some of these causes are

- Transformer energization, capacitor or feeder switching.
- Power electronic loads such as uninterrupted power supply (UPS), adjustable speed drives (ASD), converters etc.
- Arc furnaces and induction heating systems.
- Switching on or off of large loads.

2.1.1. Voltage Sag

A voltage sag is defined as a decrease in RMS voltage magnitude lasting from 0.5 to 30 cycles. Voltage sags are usually caused by a fault in the utility transmission or distribution system. Power-line faults can be due to animals in lines, cars striking utility pole, or lightning strikes to power lines. While proper maintenance and grounding and arrester location can minimize the number of faults, these phenomena can never be eliminated (Alto, 2000b). Equipment sensitivity to voltage sag occurs randomly and has become the most serious power quality problem affecting many industries and commercial customers presently. An industrial monitoring program determined an 87% of voltage disturbances could be associated to voltage sags. Most of the faults on the utility transmission and distribution system are single line-to-ground faults (SLGF) (Kreidi).

According to IEC-61000-4-30, as shown in Figure 2.1 a voltage sag event is characterized by its magnitude, which is the lowest RMS voltage during the event, and its duration, which is the time that the RMS voltage stays below the threshold (Beaulieu et al., 2002). Thus, the dip magnitude is defined the residual voltage during the sag. The power systems faults not only cause a drop in voltage magnitude but also cause change in the phase-angle of the voltage. The voltage sag duration depends on the fault clearing time. The parameters used to characterize voltage sag are magnitude, duration and phase angle jump.

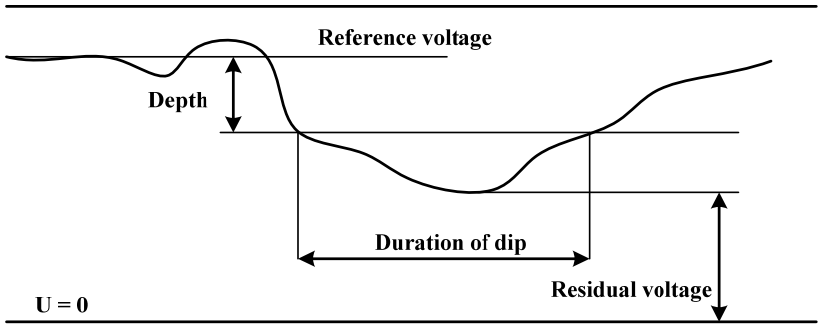


Figure 2.1. Characteristics of voltage sag

Figure 2.2 shows a basic model for calculating the magnitude of voltage sag during a three-phase fault on a radial system. Where Z_s is the source impedance at the PCC and Z_F is the impedance between the PCC and the fault.

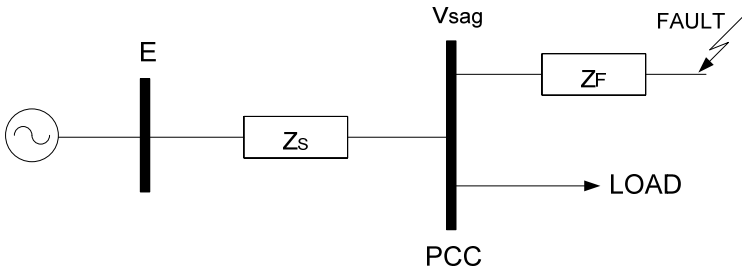


Figure 2.2. Voltage divider model for sag magnitude calculation

The current through the load before and during the fault is negligible, thus the voltage at the PCC is calculated with Equation (2.1).

$$V_{sag} = \frac{Z_F}{Z_S + Z_F} E \tag{2.1}$$

We will assume that the pre-event voltage is exactly 1 pu, thus $E = 1$. This result in the following expression for the sag magnitude.

$$V_{sag} = \frac{Z_F}{Z_S + Z_F}$$

2.1.2. Voltage Swell

As shown in Figure 2.3, swell is an increase in RMS voltage or current at the power frequency to between 1.1 and 1.8 pu for durations from half cycle and one minute as defined by IEEE Standard 1159-1995, IEEE Recommended Practice for Monitoring Electric Power Quality. Caused by system faults, load switching and capacitor switching, insulation breakdown, open neutral connection. It causes data loss, flickering of lighting and screens, stoppage or damage of sensitive equipment.

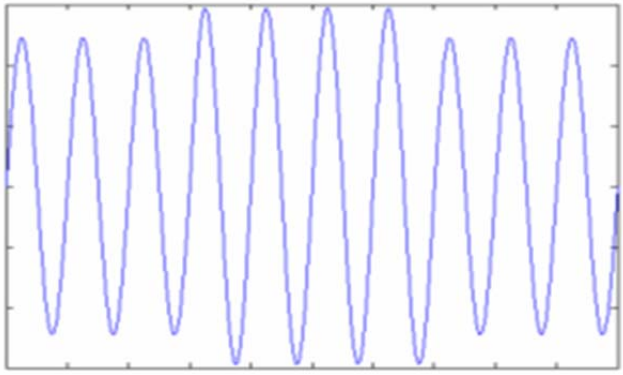


Figure 2.3. Waveform of swell

Swells are characterized by their magnitude (RMS) and duration. The severity of a voltage swell during a fault condition is a function of the fault location, system impedance and grounding. On an ungrounded system, with an infinite zero-sequence impedance, the line-to-ground voltages on the ungrounded phases will be 1.73 pu during an SLG fault condition. Close to the substation on a grounded system, there will be little or no voltage rise on the unfaulted phases because the substation transformer is usually connected delta-wye, providing a low-impedance zero-sequence path for the fault current (Dugan et al., 2004).

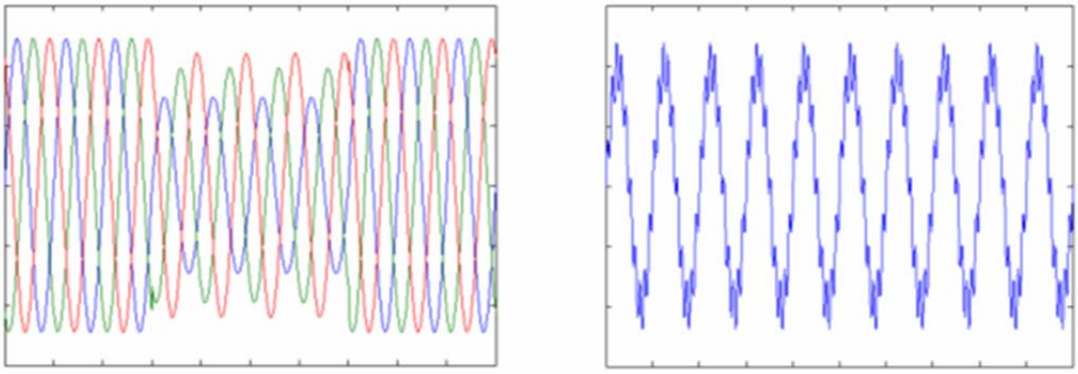
2.1.3. Voltage and Current Unbalance

Voltage/current unbalance is a condition in which the maximum deviation from the average of the three-phase voltages or currents, divided by the average of the three-phase voltages or currents, expressed in percentage. Severe voltage unbalance greater than 5% can cause damage to sensitive equipments. It can be calculated by the formula:

$$voltage\ unbalance = 100 * \frac{max.deviation\ from\ average\ voltage}{average\ voltage}$$

$$current\ unbalance = 100 * \frac{max.deviation\ from\ average\ current}{average\ current}$$

where *average voltage(current) = (sum of voltage(current) of each phase)/3.*



(a) (b)

Figure 2.4. Waveforms of (a) unbalance (b) harmonic

2.1.4. Voltage and Current Harmonics

Harmonic distortion is the corruption of the fundamental sine wave at frequencies that are multiples of the fundamental as shown in Figure 2.4(b). In practice the actual waveforms are distorted one due to presence of harmonics. Harmonics occur at an integral multiple of the base frequency. In 3-phase system odd harmonics excluding triplen frequency are prevalent. Hence 5th, 7th, 11th and even higher order harmonics can be found in the supply waveform (Bath and Kumra, 2008). The harmonic voltage and current distortion are strongly linked with each other because harmonic voltage distortion is mainly due to non-sinusoidal load currents. Current harmonic distortion requires over-rating of series components like transformers and cables. As the series resistance increases with frequency, a distorted current will cause more losses than a sinusoidal current of the same RMS value (Bollen, 2001). Some examples of common sources of power system harmonics some of which may not cause serious problems are (Phipps et al., 1994):

1) Transformer saturation
2) Transformer inrush
3) Transformer neutral connections
4) MMF distributions in AC rotating machines
5) Electric arc furnaces

6) DC converters
7) Computer switch mode power supplies
8) Battery chargers
9) Inverters
10) Static VAR compensators
11) Variable frequency motor drives (VFD)

In order to understand the amount of harmonic distortion in non-sinusoidal voltage or current waveforms and set the limits related with harmonic distortion, some indices are defined in IEEE and IEC standards. These most used indices in harmonic limits defined IEEE and IEC standards are individual harmonic distortion (*IHD*), total harmonic distortion (*THD*) and total demand distortion (*TDD*).

IHD is used either voltage or current harmonics and defined as the ratio of RMS value of each harmonic to the RMS value of the fundamental component as given in Equation 2.2.

$$IHD_V = \frac{V_h}{V_f} \qquad IHD_I = \frac{I_h}{I_f} \tag{2.2}$$

THD is also used either voltage or current harmonics and defined as the ratio of the RMS value of the harmonic components to the RMS value of the fundamental component and expressed as given in Equation 2.3.

$$I_{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_f} \qquad V_{THD} = \frac{\sqrt{\sum_{h=2}^{\infty} V_h^2}}{V_f} \tag{2.3}$$

TDD is defined as the ratio of the RMS value of the current harmonic components to the RMS value of the maximum load (demand) current fundamental component drawn from point of common coupling (PCC) and expressed in percent as given in Equation 2.4 (Tan, 2011).

$$TDD = \frac{\sqrt{\sum_{h=2}^{\infty} I_h^2}}{I_L} * 100\% \quad (2.4)$$

In Table 2.1, the voltage distortion limit values are presented. In Table 2.2, the current distortion limits for general distribution systems are shown.

Table 2.1. Voltage distortion limits (Teke, 2011)

Bus Voltage at PCC	Individual Voltage Distortion (%)	Total Voltage Distortion THD(%)
69 kV and below	3.0	5
69 kV through 161 kV	1.5	2.5
161 kV and above	1	1.5
Note: High voltage systems can have up to 2.0 % THD where the cause is an HVDC terminal that will attenuate by the time it is tapped for a user.		

Table 2.2. Current distortion limits for general distribution systems (Teke, 2011)

Individual Harmonic Order (Odd Harmonics), h						
I_{sc}/I_L	Max. Harmonic Current Distortion for h					TDD
	h<11	11≤h<17	17≤h<23	23≤h<35	35≤h	
Below 20	4.0	2	1.5	0.6	0.3	5.0
Between 20-50	7.0	3.5	2.5	1.0	0.5	8.0
Between 50-100	10.0	4.5	4.0	1.5	0.7	12.0
Between 100-1000	12.0	5.5	5.0	2.0	1.0	15.0
Above 1000	15.0	7.0	6.0	2.5	1.4	20.0
Even harmonics are limited to 25% of the odd harmonics limit above						
Current distortions that result in dc offset, e.g., half wave converters, are not allowed						
All power generation equipment is limited to these values of current distortion, regardless of actual I_{sc}/I_L						
I_{sc}= Maximum short circuit current at PCC, I_L= Maximum demand load current (fundamental frequency component) at PCC.						

2.2. Custom Power Devices

Custom power is the employment of power electronic or static controllers in distribution systems rated at 1kV through 38kV for the purpose of supplying a level of reliability and/or power quality that is needed by electric power customers who are sensitive to power variations. Custom power devices, or controllers, include static switches, inverters, converters, injection transformers, master-control modules, and/or energy-storage modules that have the ability to perform current-interruption and voltage-regulation functions in a distribution system (Alto, 2000a).

The compensating custom power devices are used for active filtering, load balancing, power factor correction, voltage regulating (sag/ swell). These devices are mainly three types: static shunt controller, series and hybrid controller. These are also called as DSTATCOM, DVR and UPQC respectively (Gupt et al., 2012).

2.2.1. Shunt Connected Devices

In its most basic form, the distribution static synchronous compensator (DSTATCOM) configuration consists of a Voltage Source Inverter (VSI), a DC capacitor for energy storage; a coupling transformer connected in shunt with the AC system and associated control circuits. In this arrangement, the steady-state power exchange between the device and the AC system is mainly reactive. Figure 2.5 shows the schematic representation of the DSTATCOM. Regulating the amplitude of the DSTATCOM output voltage controls the reactive power exchange of the DSTATCOM with the AC system. If the amplitudes of the DSTATCOM output voltage and the AC system voltage are equal, the reactive current is zero and the DSTATCOM does not generate/absorb reactive power. If the amplitude of the DSTATCOM output voltage is increased above the amplitude of the AC system voltage, the current flows through the transformer reactance from the DSTATCOM to the AC system and the device generates reactive power (capacitive). If the amplitude of the DSTATCOM output voltage is decreased to a level below that of the AC system, then the current flows from the AC system to the DSTATCOM,

resulting in the device absorbing reactive power (inductive). Since the DSTATCOM is generating/absorbing only reactive power, the output voltage and the AC system voltage are in phase, when neglecting circuit losses. The current drawn from the DSTATCOM is 90° shifted with respect to the AC system voltage, and it can be leading (generates reactive power) or lagging (absorbs reactive power). A capacitor is used to maintain dc voltage to the inverter. An uncontrolled rectifier based six diodes used to keep the capacitor charged to the required level (Sharma et al., 2014; Barghi Latran and Teke, 2014).

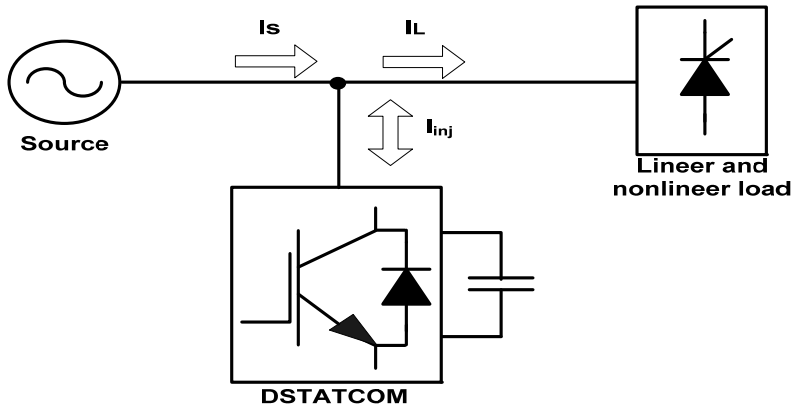


Figure 2.5. Schematic representation of the DSTATCOM

2.2.2. Series Connected Devices

The Dynamic Voltage Restorer (DVR), also referred to as the Series Voltage Booster (SVB) or the Static Series Compensator (SSC), is a device that utilizes solid state (or static) power electronic components and is connected in series to the utility primary distribution circuit (El-Gammal et al., 2011). This apparatus is suited for solving power quality problems such as voltage sags, swells, unbalance ,distortion and power factor correction. The simplified circuit of DVR is shown in the Figure 2.6.

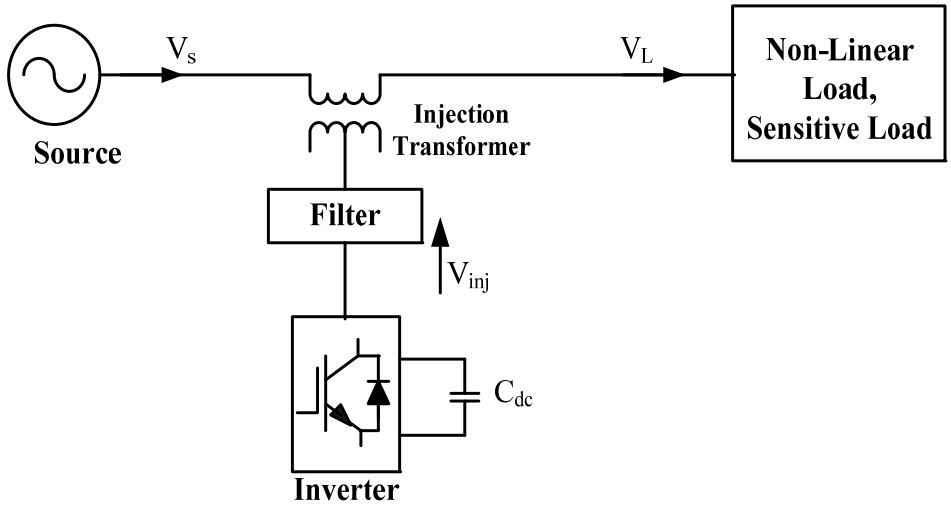


Figure 2.6. Basic components of a DVR

The basic principle of the dynamic voltage restorer is to inject a voltage of required magnitude and frequency, so that it can restore the load side voltage to the desired amplitude and waveform even when the source voltage is unbalanced or distorted. Generally, it employs a gate turn off thyristor (GTO) solid state power electronic switches in a pulse width modulated (PWM) inverter structure. The DVR can generate or absorb independently controllable real and reactive power at the load side. In other words, the DVR is made of a solid state DC to AC switching power inverter that injects a set of three phase AC output voltages in series and synchronism with the distribution line voltages (Sharanya et al., 2012; Teke, 2005).

2.2.3. Hybrid Devices

The Unified Power Quality Conditioners (UPQC) employs two voltage source inverters (VSIs) that are connected to a common dc energy storage capacitor. One of these two VSIs is connected in series with the ac line while the other is connected in shunt with the same line (Ghosh and Ledwich, 2002). Therefore it can perform both the functions of load compensation and voltage control at the same time.

The main purpose of a UPQC is to compensate for supply voltage power quality issues, such as, sags, swells, unbalance, flicker, harmonics, and for load

current power quality problems, such as, harmonics, unbalance, reactive current, and neutral current. Figure 2.7 shows a single-line representation of the UPQC system configuration (Khadkikar, 2012).

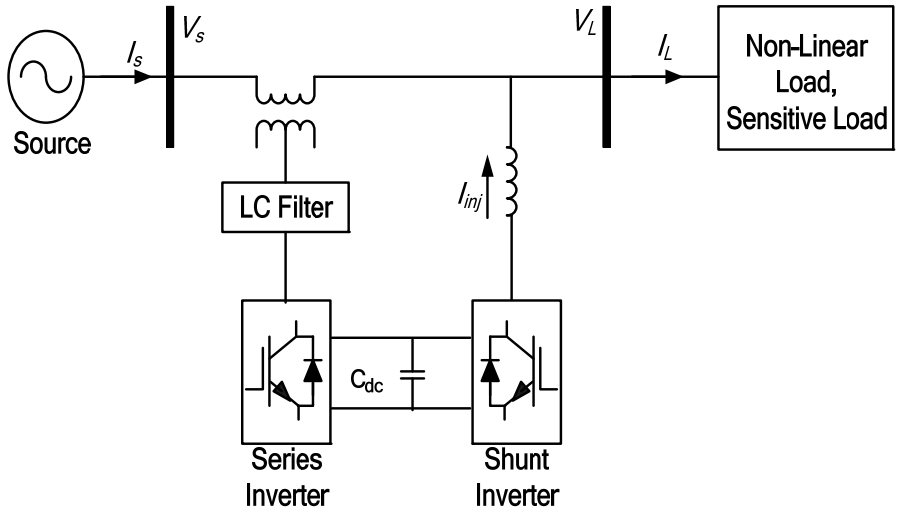


Figure 2.7. UPQC general block diagram representation

Table 2.3 is a matrix meant to give an overview of the types of events which can be mitigated by the custom power devices.

Table 2.3. Custom Power Device Application Matrix (Alto, 2000a)

	Static VAR Compensation	Static Shunt Compensation	Source Transfer Switch	Static Series Compensator	Static Voltage Regulator	Backup Energy Supply Device
Voltage Sag	✓	✓	✓	✓	✓	✓
Voltage Swell	✓	✓	✓	✓	✓	✓
Momentary Interruption			✓			✓
Capacitor Switching Transient	✓	✓		✓	✓	
Voltage Regulation	✓	✓	✓	✓	✓	
Flicker	✓	✓				
Harmonics	✓	✓				
Reactive Power Comp.	✓	✓				
Cost Range (US $)	50-200/kVAr	120 - 175/kVAr	500-1000/amp	150-250/kVA	80-125/kVA	750-1500/kVA

3. DISTRIBUTION STATIC COMPENSATOR (DSTATCOM)

3.1. Operation Principles of DSTATCOM

DSTATCOM is one of the shunt connected custom power devices and can perform load compensation, i.e., power factor correction, harmonic filtering, load balancing etc. when connected at the load terminals. It can also perform voltage regulation when connected to a distribution bus. In this mode it can hold the bus voltage constant against any unbalance or distortion in the distribution system. The DSTATCOM must be able to inject an unbalanced and harmonically distorted current to eliminate unbalance or distortions in the load current or the supply voltage (Pawar et al., 2014).

DSTATCOM system can be divided into two sections as: The power circuit and control unit. Power circuit of DSTATCOM is generally comprised an inverter (voltage source inverter is commonly preferred), DC link energy storage device, output filter and a coupling transformer as shown in Figure 3.1. Control unit consists of reference signal generation, gate signal generation, capacitor voltage balance control and voltage/current measurement.

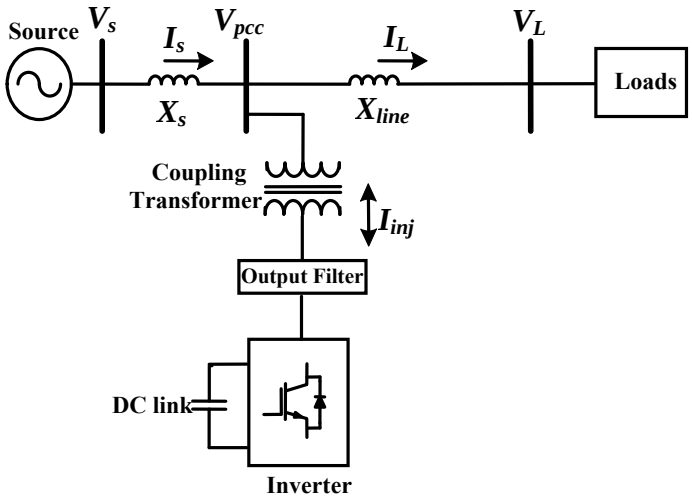


Figure 3.1. Schematic diagram of DSTATCOM.

Voltage source inverter (VSI) converts the DC voltage across the storage device into a set of three-phase AC output voltages. The generated voltages are in phase and interconnected with the utility grid through a coupling transformer. Proper adjustment of the phase and magnitude of the DSTATCOM output voltages allows effective control of active and reactive power flow between the DSTATCOM and the utility grid (Hatami et al., 2007). The single phase equivalent circuit of a power system with a DSTATCOM is shown in Figure 3.2. The V_I, $V_{Coupling}$, V_{PCC} and V_S represents the inverter output voltage; the voltage drop caused by coupling impedance, PCC voltage and source voltage, respectively.

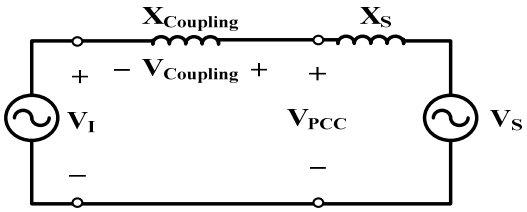


Figure 3.2. Single-phase equivalent circuit of a power system with a DSTATCOM

If V_I is equal to V_{PCC}, the exchange of reactive power between DSTATCOM and utility grid is zero and the DSTATCOM does not absorb or generate any reactive power. When V_I is greater than V_{PCC}, DSTATCOM performs an inductive reactance connected at its terminal. The current, flows through the transformer reactance from the DSTATCOM to the utility grid, and the device generates capacitive reactive power. If V_{PCC} is greater than V_I, the DSTATCOM performs the system as a capacitive reactance. Then the current flows from the utility grid to the DSTATCOM, resulting in the device absorbing inductive reactive power (Mahyavanshi et al., 2012). Figure 3.3 illustrates the V-I and V-Q characteristics of DSTATCOM which explains the reactive power exchange between DSTATCOM and utility grid.

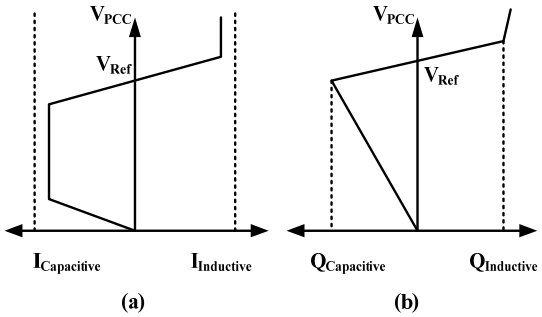


Figure 3.3. (a) V-I and (b) V-Q characteristics of the DSTATCOM

Also by proper adjustment of the phase angle between the DSTATCOM output and the utility grid voltages, the DSTATCOM can manage active power flow with the utility grid. This exchange can be used to mitigate the internal losses of the inverter and to maintain the DC capacitor charged to the proper DC voltage hereby adjusting the DSTATCOM output voltage magnitude. Figure 3.4 presents the steady state vector diagram of DSTATCOM at fundamental frequency for the transition states from inductive to capacitive mode and vice versa. The transition from capacitive to inductive mode is obtained by shifting the angle δ from zero to a positive value. The active power is transferred from the DC capacitor to the utility grid and causes a voltage drop in the DC link. The transition from inductive to capacitive mode is obtained by shifting the angle δ from zero to a negative value. The active power is transferred from the utility grid to the DC capacitor and causes a rise in the DC link voltage (Acha et al., 2002).

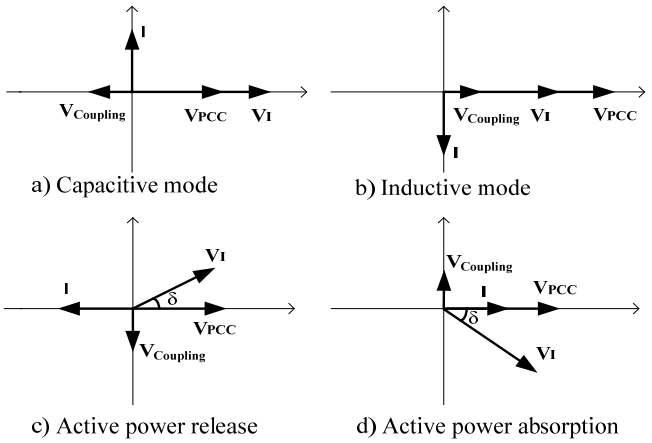


Figure 3.4. Vector diagram of DSTATCOM

The exchange of active and reactive power between DSTATCOM and utility grid can be calculated by Equation (3.1) and (3.2).

$$P = \frac{V_{PCC}\, V_I}{X_{Coupling}} \sin \delta \tag{3.1}$$

$$Q = \frac{V_{PCC}^2}{X_{Coupling}} - \frac{V_{PCC}\, V_I}{X_{Coupling}} \cos \delta \tag{3.2}$$

In practice, power losses are not negligible. The most common type of DSTATCOM losses is the combination of transformer winding and inverter switches losses. Therefore there will be a small phase angle difference between V_{PCC} and V_C to compensate the losses of transformer winding, inverter switching and draws active power from the system (Gupt et al., 2012). The power flow between the DSTATCOM and utility grid is related with DSTATCOM output voltage V_C, the utility grid voltage V_{PCC} and their phase angle differences illustrated in Table 3.1 (Acha et al., 2002).

Table 3.1. Required conditions for power exchange between DSTATCOM and utility grid

Voltage relation	Power exchange DSTATCOM	↔	Utility grid
$\|V_I\| > \|V_{PCC}\|$	Q	→	Q
$\|V_I\| < \|V_{PCC}\|$		←	
$\delta < 0$	P	→	P
$\delta > 0$		←	

3.1.1. Load Compensation

Load compensation is the management of reactive power to improve the quality of supply at a particular load or group of loads. Compensating equipment - such as power factor correction equipment- is usually installed on or near to

consumer's premises. In load compensation there are three main objectives (Acha et al., 2002):

1. Power Factor Correction and Harmonic Elimination
2. Voltage Regulation
3. Load Balancing

3.1.1.1 Power Factor Correction and Harmonic Elimination

Power factor is defined as the ratio of the active power (P) to the apparent power (S). Actually, in an ideal balanced case where there exists no harmonics; this corresponds to the cosine of the displacement angle between phase voltage and phase current. In this ideal case, reactive power (Q) can be defined as the sine of the displacement angle between phase voltage and phase current (Acha et al., 2002; Mutluer, 2008; Parlak, 2014).

$$power\ factor = \cos(\phi) = \frac{P}{S} \tag{3.3}$$

where:

$$P = Re(VI) \tag{3.4}$$

$$Q = Im(VI) \tag{3.5}$$

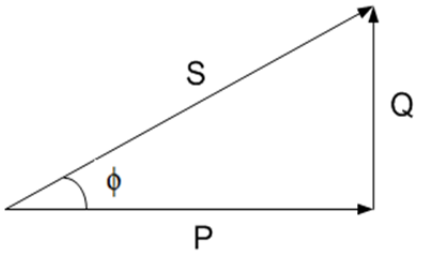


Figure 3.5. Relationship among apparent, active and reactive power

In a polyphase system, which has k phases that may also be unbalanced, the apparent power becomes:

$$S = \sum_{k} \sqrt{P_k^2 + Q_k^2}$$

Taking harmonics into account, the apparent power becomes:

$$S = \sum_{k} \sqrt{(P_k + P_{hk})^2 + (Q_k + Q_{hk})^2}$$

In equation for each phase k; P_k is the power delivered by fundamental component, P_{hk} is the power delivered by harmonic sources, Q_k is the reactive power caused by fundamental component, and Q_{hk} is the reactive power component caused by harmonics in a polyphase system. Power factor definition still holds after taking harmonics into consideration (Mutluer, 2008; Acha et al., 2002; Parlak, 2014).

Consider a single phase system shown in Figure 3.6(a) shown below. The load admittance is represented:

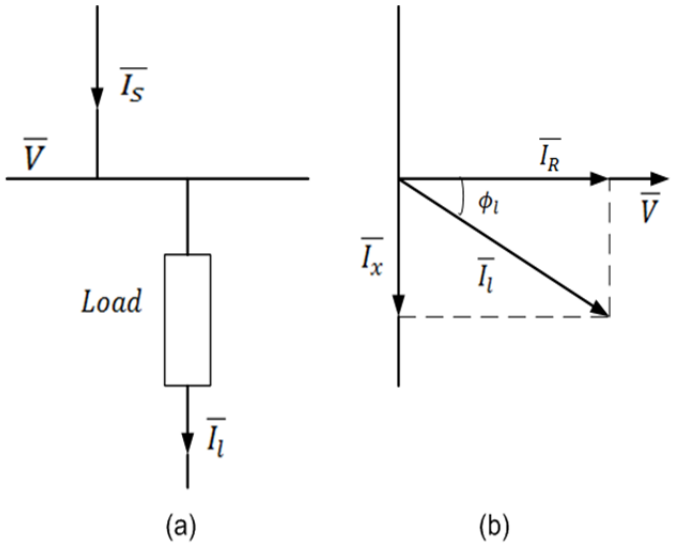


Figure 3.6. (a) Single line diagram (b) Phasor diagram of electrical system

by $Y_l = G_l + jB_l$ supplied from a load bus at voltage $\overline{V} = V\angle 0$. The load current is $\overline{I_l}$ is given as,

$$\begin{aligned}\overline{I_l} &= \overline{V}(G_l + jB_l) = VG_l + jVB_l \\ &= I_R + jI_X\end{aligned} \tag{3.6}$$

According to the above equation, the load current has a two components, i.e. the resistive or in phase component and reactive component or phase quadrature component are represented by I_R and I_X respectively. The current, I_X will lag 90˚ for inductive load and it will lead 90˚ for capacitive load with respect to the reference voltage phasor. This is shown in 3.6(b). The load apparent power can be expressed in terms of bus voltage V and load current $\overline{I_l}$ as given below.

$$\begin{aligned}\overline{S_l} &= \overline{V}(\overline{I_l})^* \\ &= V(I_R + jI_X)^* \\ &= V(I_R - jI_X) \\ &= V(I_l cos\phi_l - jI_l \sin\phi_l) \\ &= VI_l cos\phi_l - jVI_l \sin\phi_l \\ &= S_l cos\phi_l - jS_l \sin\phi_l\end{aligned} \tag{3.7}$$

From equation (3.6), $\overline{I_l} = \overline{V}(G_l + jB_l) = VG_l + jVB_l$, equation (3.7) can also be written as following:

$$\begin{aligned}\overline{S_l} &= \overline{V}(\overline{I_l})^* \\ &= V(VG_l + jVB_l)^* \\ &= V(VG_l - jVB_l) \\ &= V^2G_l - jV^2B_l) \\ &= P_l - jQ_l\end{aligned} \tag{3.8}$$

From equation (3.8), load active (P_l) and reactive power (Q_l) are given as,

$$\begin{aligned}P_l &= V^2G_l \\ Q_l &= -V^2B_l\end{aligned} \tag{3.9}$$

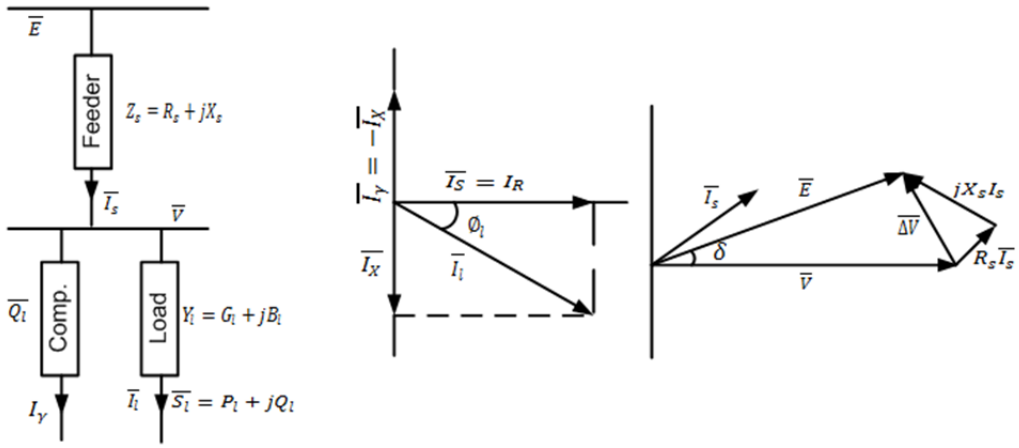


Figure 3.7. (a) Single line diagram of compensated system , phasor diagram for (b) currents, (c) voltages

Now suppose a compensator is connected across the load such that the compensator current, $\overline{I_Y}$ is equal to $-I_X$, thus,

$$\begin{aligned}\overline{I_Y} &= \overline{V}Y_Y = V(G_Y + jB_Y) \\ &= -I_X = -jVB_l\end{aligned} \tag{3.10}$$

The above condition implies that $G_Y = 0$ and $B_Y = -B_l$. The source current I_s, can therefore given by,

$$\overline{I_s} = \overline{I_l} + \overline{I_Y} = I_R \tag{3.11}$$

Therefore due to compensator action, the source supplies only in phase component of the load current. The source power factor is unity. This reduces the rating of the power conductor and losses due to the feeder impedance. The rating of the compensator is given by the following expression.

$$\begin{aligned}\overline{S_Y} &= (P_Y + jQ_Y) = \overline{V}(\overline{I_Y})^* \\ &= \overline{V}(-jVB_l)^* \\ &= jV^2B_l\end{aligned} \tag{3.12}$$

Using equation (3.9), the above equation indicates the $P_\gamma = 0$ and $Q_\gamma = -Q_l$. This is an interesting inference that the compensator generates the reactive power which is equal and opposite to the load reactive and it has no effect on active power of the load. This is shown in Fig. 3.7(b). Using (3.7) and (3.12), the compensator rating can further be expressed as,

$$Q_\gamma = -Q_l = -S_l sin\phi_l = S_l\sqrt{1 - cos^2\phi_l}\ VAr \tag{3.13}$$

From (3.13),

$$\left|Q_\gamma\right| = S_l\sqrt{1 - cos^2\phi_l} \tag{3.14}$$

3.1.1.2. Voltage Regulation

AC transmission lines are electrical networks that can be characterized mainly by per-unit series inductances and shunt capacitances. Any change in the load and load power factor results in voltage alterations along the transmission line which may lead to large amplitude differences in the sending and receiving ends. Electrical loads are usually not tolerant to voltage variations. Undervoltage conditions result in degradation of performance whereas overvoltage causes magnetic saturation and causes harmonics as well as failures because of insulation breakdown. In the extreme case, a large load change may cause the receiving end voltage to collapse, which is defined as voltage instability (Mutluer, 2008).

Voltage change from supply to load can be expressed as by showing phasors:

$$\overline{\Delta V} = \overline{E} - \overline{V} = Z_s\overline{I_l} \tag{3.15}$$

In order to regulate the voltage and mitigate voltage sag/swell, the compensator needs to alter the voltage at the load terminals which satisfies the condition $|\overline{E}|=|\overline{V}|$. After the addition of the compensator, the reactive power

becomes $Q_s = Q_\gamma + Q_l$ which is composed of compensator and load reactive power respectively. Load active power is assumed to be constant and it is denoted by P_l.

Assuming that the compensator is purely reactive:

$$= (R_S + jX_S)\left[\frac{P_l - jQ_l}{\overline{V}}\right] \tag{3.16}$$

$$= \frac{(R_S P_l + jX_S Q_l)}{\overline{V}} + \frac{(X_S P_l + jR_S Q_l)}{\overline{V}} \tag{3.17}$$

Rewriting the phasor equations,

$$\left|\overline{E}\right|^2 = \left[\overline{V} + \frac{(R_S P_l + jX_S Q_l)}{\overline{V}}\right]^2 + \left[\frac{(X_S P_l + jR_S Q_l)}{\overline{V}}\right]^2 \tag{3.18}$$

In order to find the solution where $|\overline{E}|=|\overline{V}|$, we need to solve the above equation for Q_s assuming the active power is constant at the load for the voltage variation:

$$Q_S = \frac{-2V_l^2 X_S \pm \sqrt{4\overline{V^4}X_S^2 - 4(R_S^2 + X_S^2)\left[(\overline{V^2}+R_S P_l)^2 + X_S^2 P_l^2 - \overline{E^2}\ \overline{V^2}\right]}}{R_S^2 + X_S^2} \tag{3.19}$$

This proves that there exists a solution for complete voltage regulation; however, load compensation cannot be achieved since Q_s is not zero (Mutluer, 2008; Parlak, 2014).

Looking at equation (3.19), it is seen that there exists a solution for Q_S independent of the value of P_l. Then the necessary compensator power can be found by subtracting the reactive power of the load from Q_S. For compensated load, vector diagram is given in Figure 3.7(c). It should be noted that load voltage phase is not controlled; only magnitude is under control.

According to power factor correction control algorithm, Q_S should be zero. In that case, equation (3.17) becomes

$$\overline{\Delta V} = (R_s + jX_S)\left[\frac{P_l}{V}\right] \tag{3.20}$$

Therefore, voltage regulation goes out of the compensator control as there is no related term in the equation. This proves, compensator cannot be used in both control types. In other words, a compensator cannot maintain power factor correction and voltage regulation at the same time (Parlak, 2014).

3.1.1.3 Load Balancing

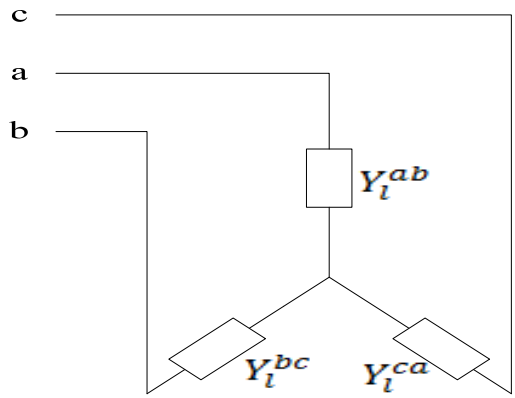


Figure 3.8. Three phase unbalanced load

In Figure 3.8, a network of Y connected admittances is given. It is clear that there exists an unbalance if Y_l^{ab}, Y_l^{bc} and Y_l^{ca} are complex and unequal. In order to balance the load, it is necessary to balance or eliminate the reactive components. By connecting a compensator parallel to each phase (Denoted by B_k^{ab}, B_k^{bc} and B_k^{ca}) imaginary component of the admittance can be eliminated as seen in Figure 3.9 (Mutluer, 2008; Acha et al., 2002).

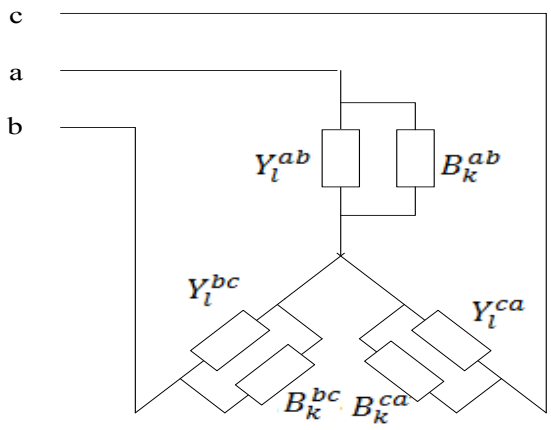


Figure 3.9. Eliminating the susceptance, thus eliminating the reactive power

In order to make admittance purely real the negative of the phase susceptance B_l^{ab} is connected parallel to the phase admittance:

$$Y_l^{ab} = G_l^{ab} - jB_l^{ab} \tag{3.21}$$

Therefore, the compensator susceptance B_γ^{ab} is:

$$B_\gamma^{ab} = -B_l^{ab} \tag{3.22}$$

The load given in Figure 3.10 will further be balanced by using the same compensator. Each phase will be balanced individually; hence, we will focus on a single phase.

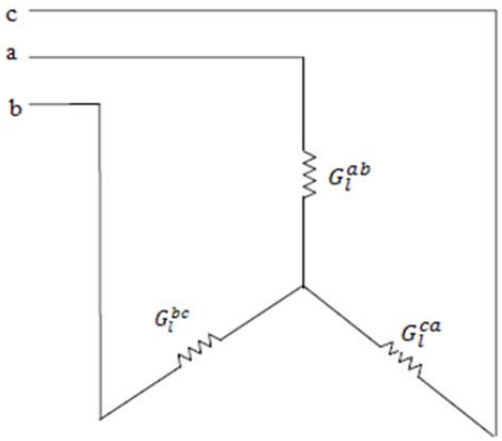


Figure 3.10. Unbalanced load with unity power factor

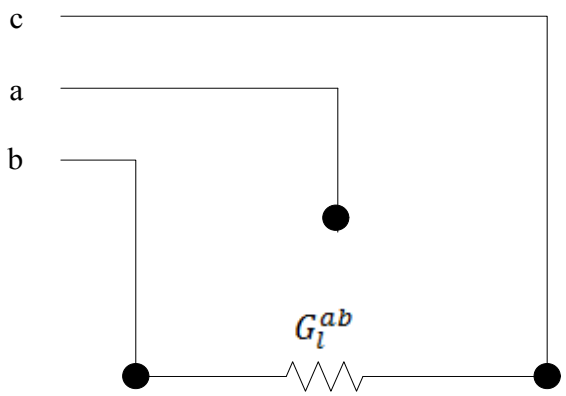


Figure 3.11. Single phase unbalanced load with unity power factor

In order to balance the real load, we will add a capacitive susceptance between the phases b and c:

$$B_\gamma^{ab} = \frac{G_l^{ab}}{\sqrt{3}} \tag{3.23}$$

In addition to this, we will add the following inductive susceptance between the phases a and c:

$$B_\gamma^{ab} = -\frac{G_l^{ab}}{\sqrt{3}} \tag{3.24}$$

The circuit becomes as seen in Figure 3.12.

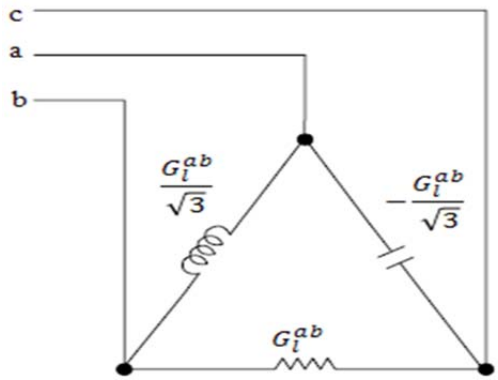


Figure 3.12. Positive sequence balancing of the single-phase unity power factor load

By making a Delta-Wye transformation of the circuit:

$$\frac{1}{Y_a} = \frac{\frac{1}{Y_{ab}} \times \frac{1}{Y_{ca}}}{\frac{1}{Y_{ab}} + \frac{1}{Y_{ca}} + \frac{1}{Y_{ba}}} \tag{3.25}$$

$$\frac{1}{Y_a} = \frac{\frac{1}{G_l^{ab}} \times \frac{1}{j\frac{G_l^{ab}}{\sqrt{3}}}}{\frac{1}{G_l^{ab}} + \frac{1}{j\frac{G_l^{ab}}{\sqrt{3}}} + \frac{1}{-j\frac{G_l^{ab}}{\sqrt{3}}}} \tag{3.26}$$

$$\frac{1}{Y_a} = \frac{\sqrt{3}}{-jG_l^{ab}} \tag{3.27}$$

$$Y_a = \frac{-jG_l^{ab}}{\sqrt{3}} \tag{3.28}$$

Similarly:

$$Y_b = \frac{jG_l^{ab}}{\sqrt{3}} \tag{3.29}$$

$$Y_c = \frac{G_l^{ab}}{3} \tag{3.30}$$

For a symmetrical components transformation, the transformation matrix is:

$$C = \frac{1}{\sqrt{3}} \begin{bmatrix} 1 & 1 & 1 \\ 1 & h & h^2 \\ 1 & h^2 & h \end{bmatrix} \tag{3.31}$$

$$C^* = \frac{1}{\sqrt{3}}\begin{bmatrix}1 & 1 & 1\\ 1 & h^2 & h\\ 1 & h & h^2\end{bmatrix} \tag{3.32}$$

where $h = e^{j2\pi/3}$

Since:

$$V = ZI \tag{3.33}$$

$$V' = C^*ZCI' \tag{3.34}$$

Assuming that Z_a, $Z_b$and Z_c are the complex impedances of the three phases, the symmetrical components impedance matrix becomes:

$$Z = \frac{1}{3}\begin{bmatrix}Z_a + Z_b + Z_c & Z_a + hZ_b + h^2Z_c & Z_a + h^2Z_b + hZ_c\\ Z_a + hZ_b + h^2Z_c & Z_a + Z_b + Z_c & Z_a + hZ_b + h^2Z_c\\ Z_a + h^2Z_b + hZ_c & Z_a + h^2Z_b + hZ_c & Z_a + Z_b + Z_c\end{bmatrix} \tag{3.35}$$

If negative sequence and zero sequence voltages are zero in the supply, the positive sequence voltage $V^+$is written in terms of current sequence components I^+, I^- and I^0 (positive, negative and zero sequence respectively):

$$\begin{bmatrix}V^+\\ 0\\ 0\end{bmatrix} = \frac{1}{3}\begin{bmatrix}Z_a + Z_b + Z_c & Z_a + hZ_b + h^2Z_c & Z_a + h^2Z_b + hZ_c\\ Z_a + hZ_b + h^2Z_c & Z_a + Z_b + Z_c & Z_a + hZ_b + h^2Z_c\\ Z_a + h^2Z_b + hZ_c & Z_a + h^2Z_b + hZ_c & Z_a + Z_b + Z_c\end{bmatrix}\begin{bmatrix}I^+\\ I^-\\ I^0\end{bmatrix} \tag{3.36}$$

Therefore for the positive sequence:

$$[V^+] = [Z_a + Z_b + Z_c \quad Z_a + hZ_b + h^2Z_c \quad Z_a + h^2Z_b + hZ_c]\begin{bmatrix}I^+\\ I^-\\ I^0\end{bmatrix} \tag{3.37}$$

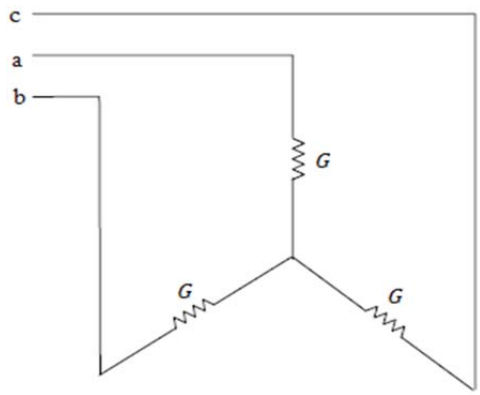
Substituting the equation (3.28),(3.29) and (3.30) into (3.37):

$$V^{+} = \frac{1}{3}\left[\frac{3}{G_l^{ab}} + \frac{\sqrt{3}}{jG_l^{ab}} - \frac{\sqrt{3}}{jG_l^{ab}}\right] I^{+} \tag{3.38}$$

The circuit becomes a wye circuit in Figure 3.13 for the positive sequence voltages and positive sequence current I^{+}eventually becomes:

$$G_l^{ab} V^{+} = I^{+} \tag{3.39}$$

Evaluating this operation for all three unbalanced phases, we get a balanced three phase system as seen in Figure 3.13.



$$G = G_l^{ab} + G_l^{bc} + G_l^{ca}$$

Figure 3.13. Positive sequence wye equivalent of the single phase unity power factor load

Therefore, the phasor diagram for the positive sequence becomes balanced. Assuming that there exists no negative sequence and no zero sequence components in the source voltage, only the positive sequence currents will flow (Figure 3.14):

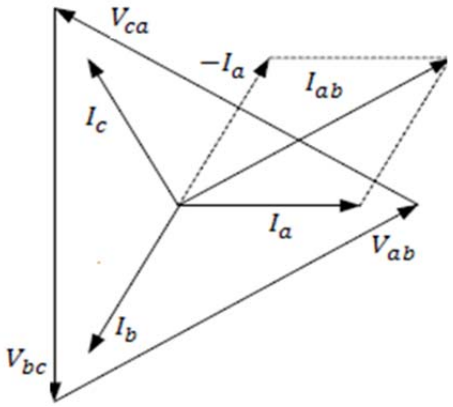


Figure 3.14. Positive sequence phasor diagram of the single phase unity power factor load

It is important to note that the overall power is still $G_{ab}|V|^2$, where $|V|$ is the amplitude of the line-to line voltage. The added inductance and reactance cause reactive power to flow through the delta; however, they cancel each other when observed from outside the delta (Mutluer, 2008; Acha et al., 2002).

3.2. Classifications of DSTATCOMs based on Power Circuit Structure

3.2.1. Classification according to the Inverter Topology

DSTATCOM converts the DC power across the storage device into a set of three-phase AC voltage or currents. To provide a fast and stable react in transient conditions, DC link value must be equal to the set reference value. The inverter is responsible to regulate the DC link voltage or current at a set reference value. DSTATCOM can be formed with a PWM current source inverter (CSI) (Bilgin and Ermiş, 2010;2011), which uses a common inductor L_{DC} to develop the DC bus. Figure 3.15 shows the configuration of CSI-based DSTATCOM system which has the advantages of its inherent boost characteristics, longer lifetime of the storage device, fault protection capability and direct control of the output current (Bai et al., 2007). Higher conduction losses of employed inductors as energy storage devices in CSI based DSTATCOM is the main reason of the CSI topology not becoming as popular configuration (Melin et al., 2008). However, with the development of

Superconducting Magnetic Energy Storage (SMES) technologies, the problem related to conventional inductors are going to be solved and hence CSIs can be considered appropriate for high power application. Moreover, the recently introduced Reverse Blocking IGBT has eliminated the need for series diode and thus making CSI a good alternative (Dash and Kazerani, 2011; 2012).

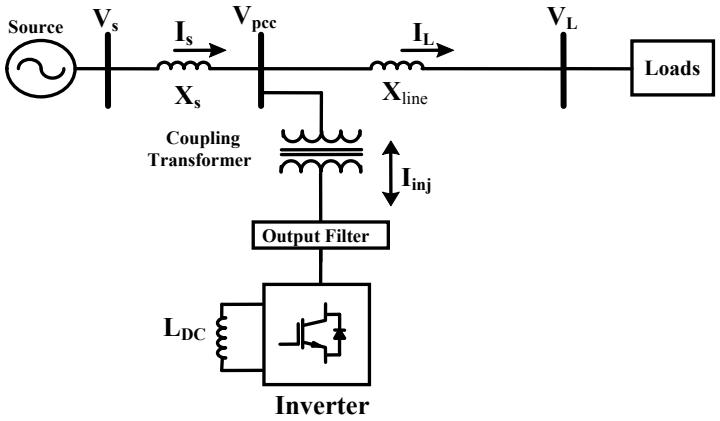


Figure 3.15. CSI based DSTATCOM configuration.

The second topology, a most popular and common inverter topology for DSTATCOM, is PWM VSI that uses a common capacitor C_{DC}. Figure 3.1 shows single-line configuration of a VSI based DSTATCOM. VSI topology is no need of blocking diodes, lighter in weight, flexible control and cheaper than CSI topology.

3.2.2. Classification according to type of Power Source

Generally, AC loads on the power system can be classified into single-phase and three-phase, according to supplied by single-phase (2-wire) or three-phase (3-wire or 4-wire) source, respectively. To mitigate PQ disturbances from the system, various DSTATCOM configurations are introduced and can be classified based on the type of the supply system configurations are used. The voltage related PQ disturbances have similar characteristics for both single-phase and three-phase systems. Additionally three-phase systems need voltage unbalance compensation

capability to satisfy enhanced PQ. In single-phase systems, reactive power and current harmonics are the main drawback. In the case of a three-phase three-wire (3P3W) system, one must consider the current unbalance expected from the reactive current and current harmonics. Additionally in the case of three-phase four-wire (3P4W) system, an extra neutral current compensation loop should be applied to eliminate the natural current (Khadkikar, 2012).

Figure 3.16 shows the most common DSTATCOM configuration consisting of two H-bridge inverters in single-phase 2-wire (1P2W) system to mitigate the PQ disturbances (Shokri et al., 2014; Perera et al., 2012). Apart from nonlinear loads fed from 3P3W system, such as adjustable speed drives, AC–AC converters, arc welding devices, and arc furnaces, cause several PQ problems. A most preferred 3P3W VSI-based DSTATCOM configuration is shown in Figure 3.17. Furthermore, three-phase loads and some industrial facilities often consist of combined loads such as a variety of single-phase and three-phase loads supplied by 3P4W source (Barghi Latran et al., 2015).

In 3P4W distribution system, the neutral line current has major role in unbalanced supply system. Generally, its value can take up to 1.73 times of phase current (Gruzs, 1990). Thus, fourth wire can cause an additional neutral line current flow and need extra compensation requirement. To eliminate the neutral line current in 3P4W system, different DSTATCOM configurations have been applied, mainly, two split capacitor (2C) (Kumar and Mishra, 2013), four-leg (4L) (George and Mishra, 2009; Kishore et al., 2012) and three H-bridge (3HB) (Ghosh and Ledwich, 2003; Elnady and Salama, 2005). In 2C topology, DC-link consists of two capacitors which are connected in split as shown in Figure 3.18. The midpoint of the capacitors provides a connection point for the fourth wire. In this topology, to prevent the flow of circulating current in the fourth wire, the voltages on the capacitors must be kept equal. For this aim, additional control loop is required to balance the capacitor voltages.

Furthermore, in DSTATCOM systems, different connection types of coupling transformer can be applied for the neutral line current compensation. Some of the connections used for eliminate the neutral line current are star-delta (Masdi et al.,

2009; Cetin and Ermis, 2009), zig-zag (Jayaprakash et al., 2012), T-connection (Singh et al., 2008) and etc.

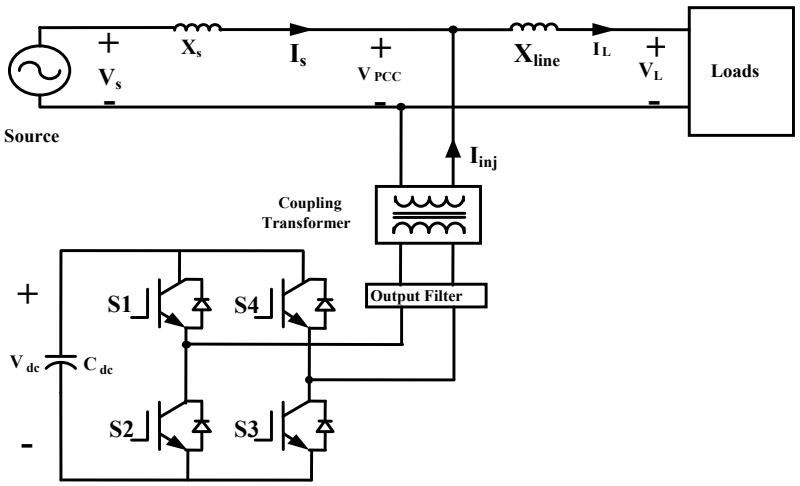


Figure 3.16. 1P2W VSI based DSTATCOM configuration.

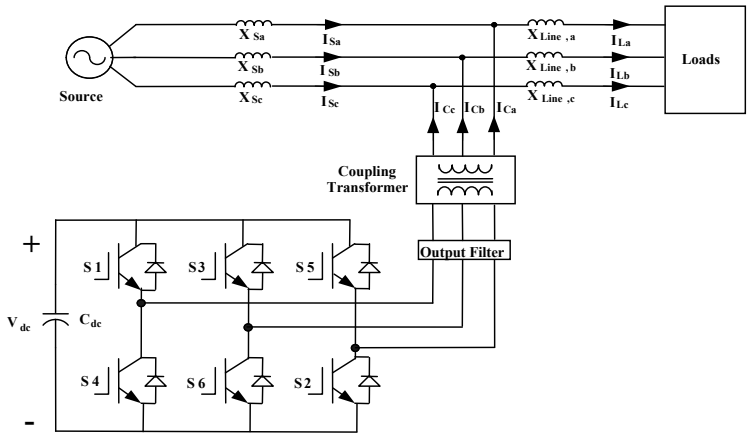


Figure 3.17. 3P3W VSI based DSTATCOM configuration.

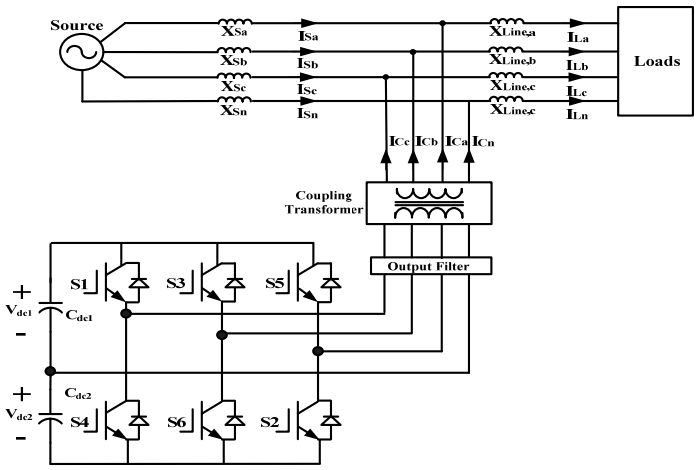


Figure 3.18. 2C inverter based 3P4W DSTATCOM configuration

3.3. Classification of DSTATCOMs Based on Control Techniques

Control strategy is the heart of the DSTATCOM and is realized in three steps. In the first step, the voltage and current signals are sensed to obtain accurate system parameters. In the second step, compensating commands in terms of current or voltage are produced based on control algorithms and DSTATCOM configurations. These control algorithms can be mainly classified into time domain methods and frequency domain methods. In the third step, the gating signals for the power switches are produced using PWM, hysteresis, sliding-mode, deadbeat or ADALINE based control techniques. The control of the DSTATCOM is performed using digital devices or advanced microelectronic devices, such as single-chip microcomputers, DSP's, FPGA's, etc. (Singh, 1999).

3.3.1. Reference Signal Extraction Techniques

The development of real-time methods and instruments for the detection and analysis of disturbances is at present a major concern in PQ analysis in order to assess the quality of supply voltage and to prevent the harmful effects on equipment. The performance of a DSTATCOM strictly depends on its reference signal generation technique. In general, frequency-domain and time-domain methods are used to generate the reference signal. The time-domain methods are faster and easy

to implement than the frequency-domain methods but they present worse detection performance than the frequency-domain methods.

- ✓ Frequency-domain methods: Frequency-domain methods are suitable for both single and three-phase systems. They are mainly derived from the Fourier analysis and include Fast Fourier Transform (FFT) (Shan et al., 2010; Singh, 1999) Kalman Filter (Gruzs, 1990; Elnady and Salama, 2005), Wavelet transform base algorithm (Ghosh and Ledwich, 2003; Lu et al., 2012).
- ✓ Time-domain methods: The following seven subdivisions of time-domain approaches are mainly used for three-phase systems. These methods are p-q theory (Kishore et al., 2012; Singh and Solanki, 2009), d-q theory (Lu et al., 2012; Geddada et al., 2012), instantaneous symmetrical component theory (Masdi et al., 2009; George and Mishra, 2009), neural network (NN) based theory (Arya et al., 2012; 2014), synchronous detection theory (Nair et al., 2012), cross vector theory (Kummari et al., 2012), back propagation (BP) based theory (Singh and Arya, 2014).
- ✓ Other algorithms: There are numerous optimization and estimation techniques such as ADALINE (Adaptive Linear Neuron) (Singh and Solanki, 2009), LMS based ADALINE (Singh and Solanki, 2011), differential evolution (Jazebi et al., 2011), time-varying Fourier coefficient series (Qi et al., 2004), Fortescue decomposition with recursive discrete Fourier transform (RDFT) (Borisov and Ginn, 2010) based algorithms used to extract the reference signal.

3.3.2. Current Control Techniques

Generation of suitable switching signal is the most significant part of DSTATCOM's control and has a high influence on the compensation performance (Melin et al., 2008). PWM is the most reliable way of reconstructing a desired output voltage waveform. The frequency of the switching should be significantly higher than that of the desired signal for a reliable signal representation (Ghosh and Ledwich, 2002). PWM methods are often categorized as open loop (feed-forward) and closed loop (feed-back) methods. The open loop method is subdivided into

sinusoidal PWM (SPWM) (Masdi et al., 2009) and space vector PWM (SVM) (Singh et al., 1999; Saeedifard et al., 2007). The closed loop method are classified into hysteresis current control (Saeedifard et al., 2007; Gupta and Ghosh, 2006) and linear current control involving ramp comparison (Colak et al., 2011), state feedback, synchronous vector, predictive (Moon,1999), deadbeat (Kazmierkowski and Malesani, 1998), sliding mode (Jung and Tzou et al., 1993), linear quadratic regulator (Ghosh and Ledwich, 2003), pole shift controllers (Ramakrishna and Malik, 2010). Apart from these methods the selective harmonic elimination technique (Cetin and Ermis, 2009) also used for generation proper switching signal.

The classification of DSTATCOM according to compensated variables is presented in Table 3.2.

Table 3.2. Classification of DSTATCOM according to compensated variables

	Reactive Power	Voltage Regulation	Current harmonic	Voltage harmonic	Balanced Voltage Sag	Balanced Voltage Swell	Unbalanced Voltage Sag	Unbalanced Voltage Swell
(Geddada et al., 2015)	✓	✓	✓					
(Singh et al., 2015)	✓		✓	✓				
(Murugesan et al., 2015)	✓							
(Xu et al., 2015)	✓	✓	✓	✓				
(Arya and Singh 2015)	✓	✓	✓	✓				
(Suvire and Mercado,2012)	✓							
(Chen et al., 2013)	✓	✓						
(Muñoz et al., 2014)	✓		✓					
(Cetin et al., 2009)	✓		✓	✓				
(Karmiris et al., 2012)			✓		✓			
(Patil and Madhale,2007)					✓	✓	✓	
(Elnady and Salama, 2005)							✓	
(Jayaprakash et al., 2012)	✓	✓	✓					
(Venkatesh et al., 2010)			✓		✓	✓		
(Sukanth et al., 2012)	✓	✓	✓					
Proposed system	✓	✓	✓	✓	✓	✓	✓	

4. DESIGN OF PROPOSED DSTATCOM

In the thesis, the control strategy of improving DSTATCOM performs the following functions of the DSTATCOM:

1. The reactive power compensation
2. Voltage regulation
3. Compensation of voltage sag and swell
4. Compensation of load current harmonics
5. Compensation of the load unbalance

The proposed model consists of following parts to solve all problem mentioned in above:

1. Power Supply
2. Loads
3. DSTATCOM
   a. Power Circuit
      i. Voltage Source Inverter
      ii. Interface Filter
      iii. DC Link
   b. Control Circuit
      i. Reference Current Generation
      ii. Current Control

Figure 4.1 shows the main components of a typical DSTATCOM system and their interconnections.

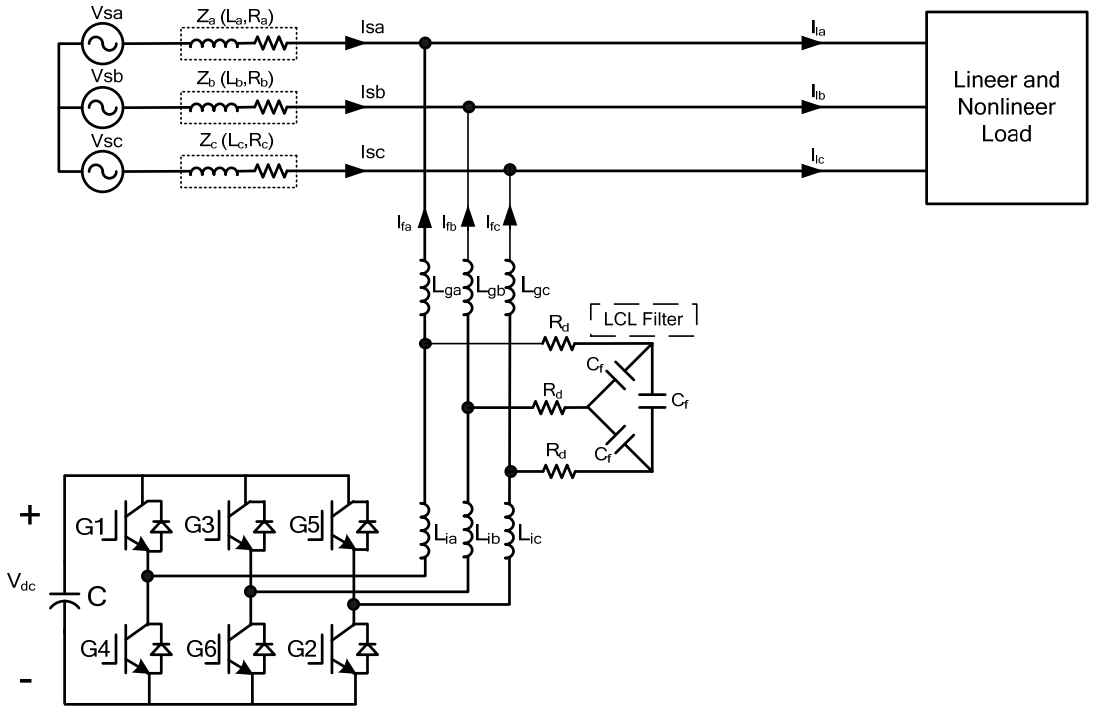


Figure 4.1. Diagram illustrating components of the DSTATCOM

4.1. Power Supply

Power supply is a Y connected 400V (L-L) at 50 Hz. For modeling the grid a symmetrical three-phase voltage source having an inductance and resistance is used.

4.2. Loads

The most important issue to be considered when a DSTATCOM is designed, total characteristic of nonlinear loads which are connected point of common connection is to be made reactive power compensation and harmonic filtering. The nonlinear load block is a three-phase fully controlled thyristor bridge rectifier feeding DC load. Loads are designed as linear and nonlinear with wye-connected three-phase three-wire systems and total rating of 300kVA (0.8 pf.).The PSCAD model of the linear and nonlinear load block is shown in Figure 4.2.

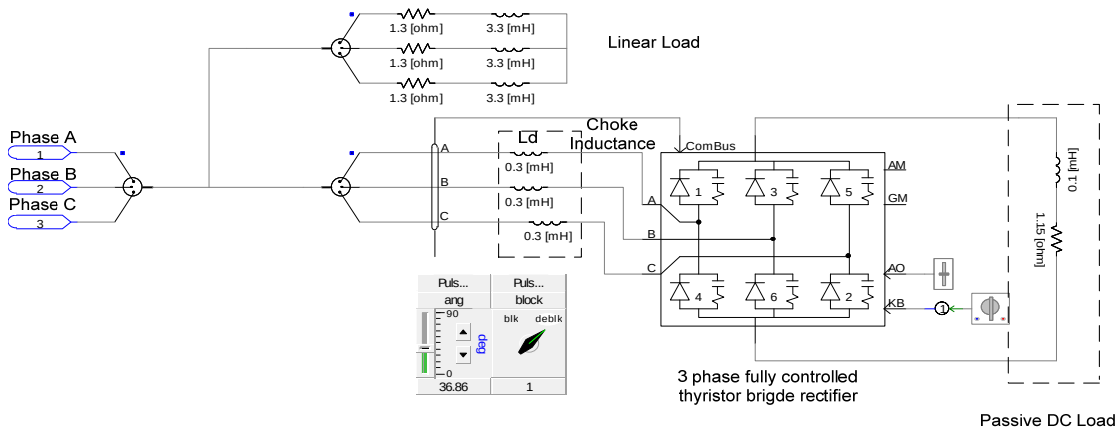


Figure 4.2. PSCAD model of the linear and nonlinear load.

Voltage drop occurs at PCC during switching commutation at the thyristor rectifier. The reason for this doesn't disconnect currents of line inductances at phase immediately. Therefore, line commutated thyristor rectifier when passing from a phase to another phase, three thyristor passes transmission simultaneous. Line to line voltage connected two of the three thyristors by-passes at PCC. In this case, in order to prevent the emerging line voltage notches, choke inductances connect AC inputs of thyristor and diode rectifier. According to German VDE standards, at the maximum fundamental load current, the voltage drop on the choke inductance should be a minimum of 5% line-neutral voltage.

$$wL_dI_L \geq 0.05\frac{V_{LL}}{\sqrt{3}} \tag{4.1}$$

w : fundamental frequency (rad/s)

L_d : choke inductance (H)

I_L : fundamental load current

V_{LL} : line to line voltage

Choke inductance value is calculated as $L_d \geq 0.085mH$ using (4.1) when $V_{LL} = 400V, I_L = 433\text{A}$ and $w = 314.16$ rad/s . The choke inductance is selected as 0.3mH.

4.3. DSTATCOM Power Circuit Configuration

4.3.1. Design of Voltage Source Inverter

The inverter circuit converts DC power to AC power. Three-phase IGBT with anti-paralleling diodes having turn-off capability are used in the inverter circuits. A voltage source inverter is energized by a capacitor at the input. The inverter is then connected in parallel to the distribution line through interface filter (LCL) as shown in Figure 4.1. The interface filter establish a link between VSI and power system.

The voltage source inverter used in DSTATCOM makes the harmonic control possible. This inverter uses a DC capacitor as the supply and can switch at a high frequency to generate a signal which will cancel the harmonics from the nonlinear load. The current waveform for canceling harmonics is achieved with the voltage source inverter and an interface filter. The interface filter converts the voltage signal created by the inverter to a current signal. The desired waveform is obtained by accurately controlling the switches in the inverter. Control of the current wave shape is limited by the switching frequency of the inverter and by the available driving voltage across the interface filter. The driving voltage across the interface filter determines the maximum *di/dt* that can be achieved by the filter. This is important because relatively high values of *di/dt* may be needed to cancel higher order harmonic components (Bayındır, 2008).

4.3.2. Design of DC Supply

A DC-link capacitor provides constant DC link voltage. The output voltage of the DSTATCOM is generated by a DC/AC voltage source converter operated from an energy storage capacitor (Udaykiran et al., 2012).

The capacitor must be pre-charged to sufficiently high value in order to obtain satisfactory tracking performance. However, increasing the capacitor voltage increases the losses in the system. Therefore, the level of capacitor voltage must be chosen judiciously [Zaveri et al., 2011]. This problem can be solved by controlling

the magnitude of mains current. A PI controller is used to control the DC capacitor voltage.

According to the above analysis, the selection of capacitor voltage (V_{dcref}) and capacitance of the capacitor value C_{DC} can be determined from (4.2) and (4.3),

$$V_{dcref} = \frac{2\sqrt{2}\, V_{LL}}{\sqrt{3} m_a} \tag{4.2}$$

$$C_{dc} = \frac{3 S_n n T}{(1.8 V_m)^2 - (1.4 V_m)^2} \tag{4.3}$$

where V_{dcref} is the reference capacitor voltage, V_{LL} is line to line grid voltage, m_a is the modulation index, C_{dc} is the DC capacitor value, V_m is peak value of grid voltage, S_n is power rate of system, T is system time period, n is the cycle that starts working the controller.

Reference DC voltage is estimated as 680V using (4.2) when m_a=1 and $V_{LL} = 400V$. DC capacitor value is calculated as 66 mF using (4.3) when $V_m = 326.6V$, $S_n = 300kVA$, $n = 0.5$ and $T = 0.02\ s$,. The capacitor is selected as 60mF.

4.3.3. Inverter Output Filter

4.3.3.1. L Filter

The L-Filter (Figure 4.3) is the first order filter with attenuation 20 dB/decade over the whole frequency range. Although a single inductor L-filter is popular and simple use, it has a low attenuation and high inductance value. The voltage drop across the inductor makes a poor system dynamics, hence causing a long-time response. By using L-filter, the inverter switching frequency must have a high value in order to sufficiently attenuate the harmonics (Cha and Vu, 2010: E-Habrouk et al., 2000).

Since the L-filter achieves low attenuation of the inverter switching components, a shunt element is needed to further attenuate the switching frequency components. A capacitor is selected to produce low reactance at the switching frequency and presents high magnitude impedance within the control frequency range (Cha and Vu, 2010).

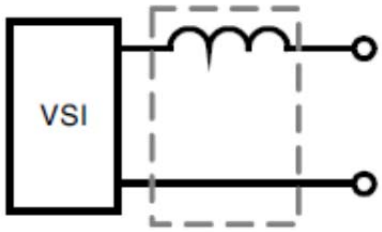


Figure 4.3. Circuit diagram of L filter

Peak ripple current is chosen to be the criterion for designing the inductor. For calculating the ripple current, no-load condition is considered and the effect inductor resistance is assumed to be negligible. Under this condition, the inverter reference voltage is equal to the supply voltage. Thus the required smoothing inductance given by (Chaoui et al., 2008):

$$L_f = \frac{V_{dc}}{6 f_{sw} \Delta_{ph(p-p)max}} \tag{4.4}$$

where $\Delta_{ph(p-p)max}$= 15% of peak compensation current, V_{dc} is the supply voltage of inverter (DC link voltage) and f_{sw} is the switching frequency. The smoothing inductance is calculated as 0.17 mH using (4.4) when V_{dc} = 680V , $\Delta_{ph(p-p)max}$= 65A and f_{sw} = 10kHz. To improve the smoothing inductance performance in simulation study, the inductance is selected as 0.15mH.

4.3.3.2. LCL Filter

The attenuation of the LCL filter is 60 dB/decade for frequencies above resonant frequency, therefore lower switching frequency for the converter can be

used. Namely, the high frequency harmonics in voltage and current, generated by the high frequency switching in the VSI, can be suppressed by the use of a LCL filter. The LCL filter consists of two inductors in series and a capacitor shunted between them. Compared to a filter with the use of a single inductor, the damping of the switching harmonics, at lower switching frequency, improve by using a LCL filter. The total inductance of the filter should be as small as possible to realize fast tracking and high dynamics, and still handle the ripple in the current (Midtsund, 2010).

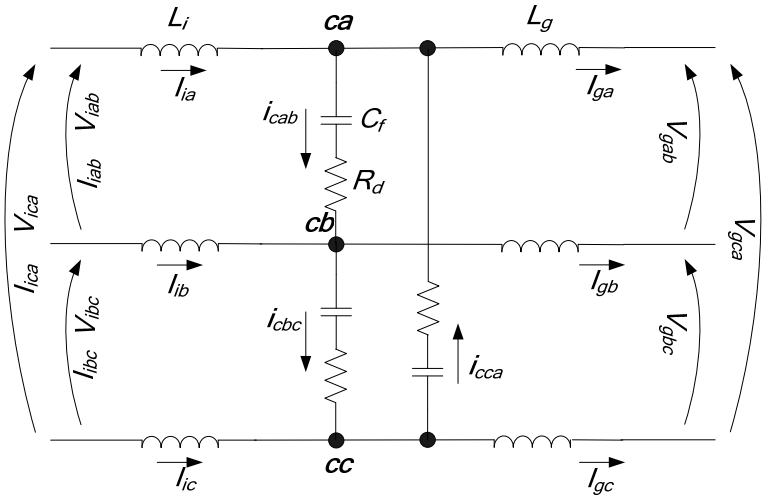


Figure 4.4. Circuit diagram of LCL Filter

Wye connected LCL filters are generally used in systems, but delta connected LCL filter is used in this thesis as shown Figure 4.4. If inductances and capacitances are the same for a delta connected LCL filter and a wye connected LCL filter, resonant frequency of a delta connected LCL filter is decreased to 3 times resonant frequency of a wye connected LCL filter. So, there are more reduced harmonics in capacitor currents in case of a delta connected LCL filter than a wye connected LCL filter. As switching frequency is lower to a few kilohertz, these harmonics cause to distort inverter control signals. Therefore, it is advantageous to control an inverter with a delta connected LCL filter because currents flowing into wye connected capacitors have harmonic components with larger magnitude (Lee et al., 2008).

From Figure 4.4:

$V_{iab}, V_{ibc}, V_{ica}$	inverter line-to-line voltages
$V_{gab}, V_{gbc}, V_{gca}$	grid line-to-line voltages
$V_{cab}, V_{cbc}, V_{cca}$	potential voltage between node ca, cb and cc
I_{ia}, I_{ib}, I_{ic}	inverter line currents flowing from the inverter side to the filter
I_{ga}, I_{gb}, I_{gc}	grid line currents flowing from the filter to the grid side
$I_{iab}, I_{ibc}, I_{ica}$	phase currents calculated from I_{ia}, I_{ib} and I_{ic}
$I_{cab}, I_{cbc}, I_{cca}$	capacitor currents
ca, cb, cc	nodes at capacitors

Applying Kirchhoff's current law and voltage law to Figure 4.4., differential equations can be achieved. These are (4.5) for paths between the inverter side and the filter, (4.6) for paths between the filter and the grid side, (4.7) at capacitors in the filter.

$$-\begin{bmatrix} V_{iab} \\ V_{ibc} \\ V_{ica} \end{bmatrix} + 3L_i \frac{d}{dt}\begin{bmatrix} I_{iab} \\ I_{ibc} \\ I_{ica} \end{bmatrix} + \begin{bmatrix} V_{cab} \\ V_{cbc} \\ V_{cca} \end{bmatrix} = 0 \tag{4.5}$$

$$-\begin{bmatrix} V_{cab} \\ V_{cbc} \\ V_{cca} \end{bmatrix} + 3L_g \frac{d}{dt}\begin{bmatrix} I_{gab} \\ I_{gbc} \\ I_{gca} \end{bmatrix} + \begin{bmatrix} V_{gab} \\ V_{gbc} \\ V_{gca} \end{bmatrix} = 0 \tag{4.6}$$

$$C_f \frac{d}{dt}\begin{bmatrix} V_{cab} \\ V_{cbc} \\ V_{cca} \end{bmatrix} - R_d C_f \frac{d}{dt}\begin{bmatrix} I_{cab} \\ I_{cbc} \\ I_{cca} \end{bmatrix} = \begin{bmatrix} I_{cab} \\ I_{cbc} \\ I_{cca} \end{bmatrix} \tag{4.7}$$

It is supposed that $[V_{iab}\ V_{ibc}\ V_{ica}]' = V_i$, $\left[V_{gab}\ V_{gbc}\ V_{gca}\right]' = V_g$, $[V_{cab}\ V_{cbc}\ V_{cca}]' = V_c$, $[I_{iab}\ I_{ibc}\ I_{ica}]' = I_i$, $\left[I_{gab}\ I_{gbc}\ I_{gca}\right]' = I_g$, $[I_{cab}\ I_{cbc}\ I_{cca}]' = I_c$ where symbol $'$ means transpose. Equation (4.5), (4.6) and (4.7) are transformed to (4.8) by the Laplace transform theorem on the assumption that all initial values of the state variables are zero. Then, desired transfer functions $I_c(s)/V_i(s)$, $V_c(s)/I_c(s)$,

and $I_2(s)/(V_c(s) - V_g(s))$ can be calculated from (4.8) to represent the system. The equation (4.9) is the proposed mathematical model of the system.

$$\begin{bmatrix} -V_i(s) + s\,3L_i I_i(s) + V_c(s) = 0 \\ -V_c(s) + s\,3L_g I_g(s) + V_g(s) = 0 \\ sC_f V_c(s) = \left(1 + sC_f R_d\right) I_c(s) \end{bmatrix} \tag{4.8}$$

$$\begin{bmatrix} G_1 = \dfrac{I_c(s)}{V_i(s)} = \dfrac{s^2 3L_g C_f}{s3\left(L_i + L_g\right) + s^2 3C_f R_d\left(L_i + L_g\right) + s^3 9L_i L_g C_f} \\ G_2 = \dfrac{V_c(s)}{I_c(s)} = \dfrac{1 + sC_f R_d}{sC_f} \\ G_3 = \dfrac{I_g(s)}{V_c(s) - V_g(s)} = \dfrac{1}{s3L_g} \end{bmatrix} \tag{4.9}$$

The first-harmonic, low order harmonic and high order harmonic current could be got by decomposing the output current of inverter. As shown in Figure 4.4, the current ripple is decreased because of inductance L_i that the current flow through. The capacitance is features low resistance to high order harmonic, but the inductance is features high resistance, so the high order harmonic can only flow through capacitance. Then the left current of first-harmonic and low order harmonic flow through inductance L_g into power grid (Renzhong et al., 2013).

Parameters design of the inductors in LCL filter is based on the principle as follows:

1. The voltage drop at the inductors of LCL filter must be less than 10% of the phase voltage of the grid.

$$w\left(L_i + L_g\right) I_N < 10\% * U_N/\sqrt{3} \Rightarrow \left(L_i + L_g\right) < 0.17\ mH$$

2. In order to limit the short circuit current and the harmonic current, the inductance of inductors should not be too small. The minimum value of inductance is determined by the ripple current which is chosen between 10%-20%.

$$20\% * 8 * (L_i + L_g) I_N f_{SW} \geq V_{DC} \Rightarrow (L_i + L_g) \geq 0.098\ mH$$

In conclusion, the value range of inductance of the inductors in LCL filter is

$$0.0098\ mH \leq L_i + L_g < 0.17\ mH$$

The value of inductance is chosen as 0.1 mH. So the inductance values are

$$L_i = 0.07\ mH, \qquad L_g = 0.03\ mH$$

In order to guarantee the efficiency of DSTATCOM, reactive power absorbed by filter capacitors must be less than 5% of rated capacity.

$$C \leq \frac{5\%\ S_n}{3w\left(\frac{V_s}{\sqrt{3}}\right)^2} \Rightarrow C \leq 0.3\ mF$$

The value of capacitance for star connection is chosen as 0.25 mF. Delta connection capacitance value is estimated as 0.083 mF.

For making the harmonics current flow through the filter capacitors as more as possible and the resonant frequency of LCL filter should avoid appearing in low or high frequency band, parameters design should meet the following requirements.

$$X_c = (0.1 : 0.2) X_{Lg}$$

$$10 f_n < f_{res} < f_c/2 \Rightarrow 0.5\ kHz < f_{res} < 5\ kHz$$

Test as follows:

$$\frac{X_c}{X_{Lg}} = \frac{1}{w_c^2 C L_g} = 0.1$$

$$f_{res} = \frac{1}{2\pi}\sqrt{\frac{L_i + L_g}{3 L_i L_g C}} = 2.2\ kHz$$

***Damping Resistance*:** The equivalent impedance of the passive *LCL*-filter approaches zero at the resonance frequency and it will consequently lower the stability margin of the system down. To avoid instability, a resistor R_d is used in series with the capacitor. The resistance R_d is normally selected in proportion to the capacitive reactance of the filter at the resonance frequency ($1 \,/\, (3 * 2\pi f_{res} C)$. This resistance can be chosen such that it minimizes the power dissipation too (Bina and Pashajavid, 2009).

Comparison of L and LCL filter performances based on various parameters is presented in Table 4.1.

Table 4.1. Comparison of L and LCL Filters

Parameters	L filter	LCL filter
Switching ripple in percentage (terminal voltages, source currents)	high	low
Value of L for ripple percentage in filter currents	large	small
Source neutral current	high	low
Compensation performance in terms of %THD	good	good
Current controller complexity	less	relatively more

4.4. DSTATCOM Control Strategy

4.4.1. Reference Current Generation

DSTATCOM control is accomplished by monitoring the three phase line currents to the linear/nonlinear loads and the three phase line-to-neutral voltages at the load bus, and then generating the three phase reference currents that should be supplied by the voltage source inverter. In this simulation study compensating current reference signal is derived from the measured quantities by the use of the Instantaneous Symmetrical Component Theory (ISCT) and Synchronous Reference Frame (SRF) based method.

When the compensating currents are detected, they are used as a reference signal in the inverter current control loop and thus compared with the real voltage source inverter current to generate the switching control signals.

Firstly, for extract the current reference signal, the positive sequence of current extract by the ISCT. The mathematical details of ISCT was mentioned in Section 3.1.1.3.

The transformation is defined as:

$$\begin{bmatrix} V^+ \\ V^- \\ V^o \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

Here V^+, V^- and V^o denote the positive, negative and zero sequences respectively and the complex number *a* is:

$$a = e^{j\frac{2\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$$
$$a^2 = e^{j\frac{4\pi}{3}} = -\frac{1}{2} + j\frac{\sqrt{3}}{2}$$

The inverse of this transformation is:

$$\begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix} = \begin{bmatrix} 1 & 1 & 1 \\ a^2 & a & 1 \\ a & a^2 & 1 \end{bmatrix} \times \begin{bmatrix} V^+ \\ V^- \\ V^o \end{bmatrix}$$

The instantaneous positive-sequence components are defined as

$$\begin{bmatrix} V_a^+ \\ V_b^+ \\ V_c^+ \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & a & a^2 \\ a^2 & 1 & a \\ a & a^2 & 1 \end{bmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

The instantaneous negative-sequence components are defined as

$$\begin{bmatrix} V_a^- \\ V_b^- \\ V_c^- \end{bmatrix} = \frac{1}{3} \times \begin{bmatrix} 1 & a^2 & a \\ a & 1 & a^2 \\ a^2 & a & 1 \end{bmatrix} \times \begin{bmatrix} V_a \\ V_b \\ V_c \end{bmatrix}$$

The instantaneous zero-sequence components are defined as

$$V_a^0 = V_b^0 = V_c^0 = \frac{1}{3}(V_a + V_b + V_c)$$

Secondly, ABC components of extracted positive sequences are transformed to the orthogonal and stationary $\alpha\beta$ frame system by used the Clarke transformation. The equation of Clarke transformation is given in Equation (4.10).

$$i_{\alpha\beta}(t) = \frac{2}{3}\begin{bmatrix} 1 & -\frac{1}{2} & -\frac{1}{2} \\ 0 & \frac{\sqrt{3}}{2} & -\frac{\sqrt{3}}{2} \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{4.10}$$

Next step, the stationary components of the currents convert to direct (d) and quadrature (q) components by Park's transformation The values of DQ transformation are calculated using (4.11). The phase angle θ defines the fundamental frequency phase information of the utility voltage and it is obtained from a phase locked loop circuit which is investigated.

$$i_{dq} = \frac{2}{3}\begin{bmatrix} \cos\theta & \sin\theta \\ -\sin\theta & \cos\theta \end{bmatrix}\begin{bmatrix} i_\alpha(t) \\ i_\beta(t) \end{bmatrix} \tag{4.11}$$

$$i_{dq} = \frac{2}{3}\begin{bmatrix} \cos\theta & \cos(\theta-120) & \cos(\theta+120) \\ \sin\theta & \sin(\theta-120) & \sin(\theta+120) \end{bmatrix}\begin{bmatrix} i_a(t) \\ i_b(t) \\ i_c(t) \end{bmatrix} \tag{4.12}$$

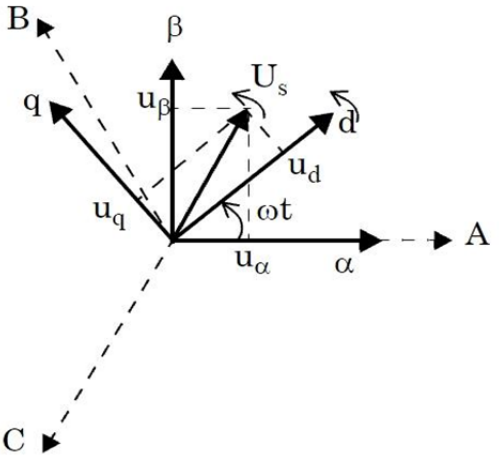


Figure 4.5. αβ and DQ rotating frame vector representation

If three-phase parameters such as currents and voltages are balanced, the value of the DQ transformation results in DC constant values. In addition, the resulting DC values make voltage controller design easier. Figure 4.5 shows three-phase voltages and their *dq*-axis values for the balanced voltage sag. Figure 4.6 shows the resulting DQ values. It is clearly shown that regardless of the voltage sag, the value in *d*-axis remains zero, and the *q*-axis component instantaneously indicates the change of the voltage magnitude. The DQ transformation uses instantaneous values. Therefore, the detection time is much faster than other methods such as average, RMS, and peak detection. However, for the unbalanced voltage sag, this DQ transformation method does not show the instant change of DC values.

Figure 4.6. The result of DQ transformation of balance three phase voltage

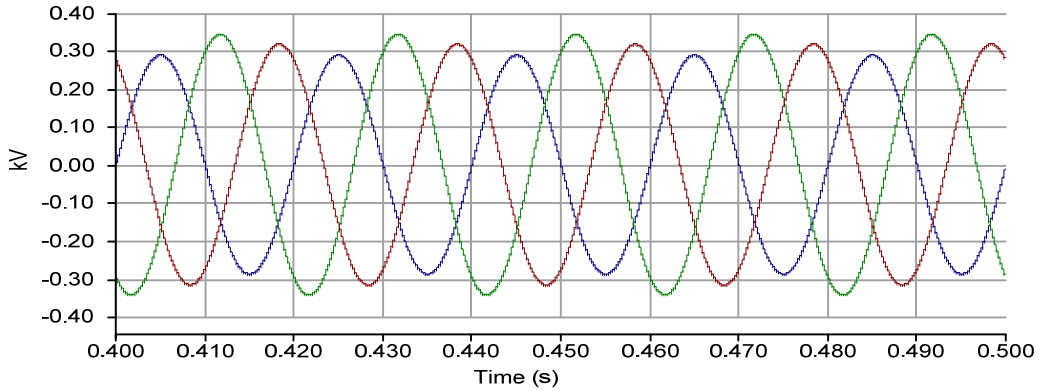


Figure 4.7. The result of DQ transformation of unbalance three phase voltage

- **AC Voltage Controller**

To control the magnitude of the voltage at PCC, an AC voltage controller using reactive power injection is used. Injection of reactive current at PCC results in a change of the voltage magnitude due to the variation of the voltage drop over the impedance of the system at PCC. V_{ac} is compared with the pre-defined reference value V_{ref}. The error signal is fed to the PI block to generate the small signal oscillation is limited to suppress the variation in the output. Figure 4.8, describes the structure of AC voltage controller.

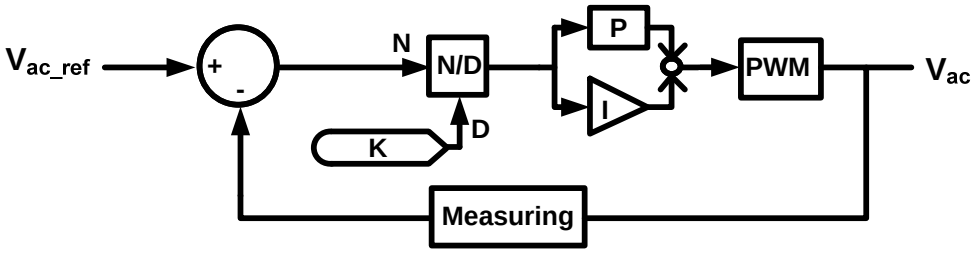


Figure 4.8. The structure of AC voltage controller

- **DC Link Voltage Controller**

What happens actually is that the DC bus loses some of its energy to compensate for the energy losses of the system and in this process its voltage starts to drop. As the voltage tries to drop, the voltage controller acts and maintains the DC

bus voltage constant by absorbing active power from the grid. Thus, the voltage controller indirectly uses the DC bus voltage (rather than measuring the actual losses in the system) to supply the energy losses of the system from the grid (Karuppaswamy, 2007).

The DC side voltage V_{dc} is measured and compared with the reference voltage side V_{dcref}, and the error signal is fed to PI controller. Figure 4.9 describes the structure of DC voltage controller.

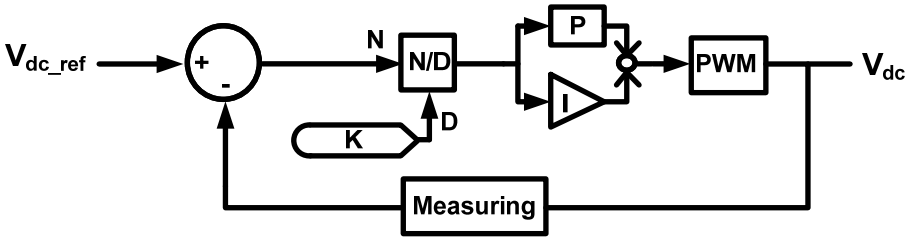


Figure 4.9. The structure of DC link voltage controller

4.4.2. PWM Current Controller

PWM switching method is used as gate signal generation for VSI. The switching pulses are generated by comparing the reference current compensation signal I_{error} with a fixed frequency carrier triangular wave. PWM switching method obtains a constant switching frequency to the power electronics devices in VSI. And the frequency of the triangular wave is set to f_{tri} = 10kHz.

4.4.3. Overall Controller of PWM-VSI

The overall control structure of DSTATCOM using PWM is shown in Figure 4.10.

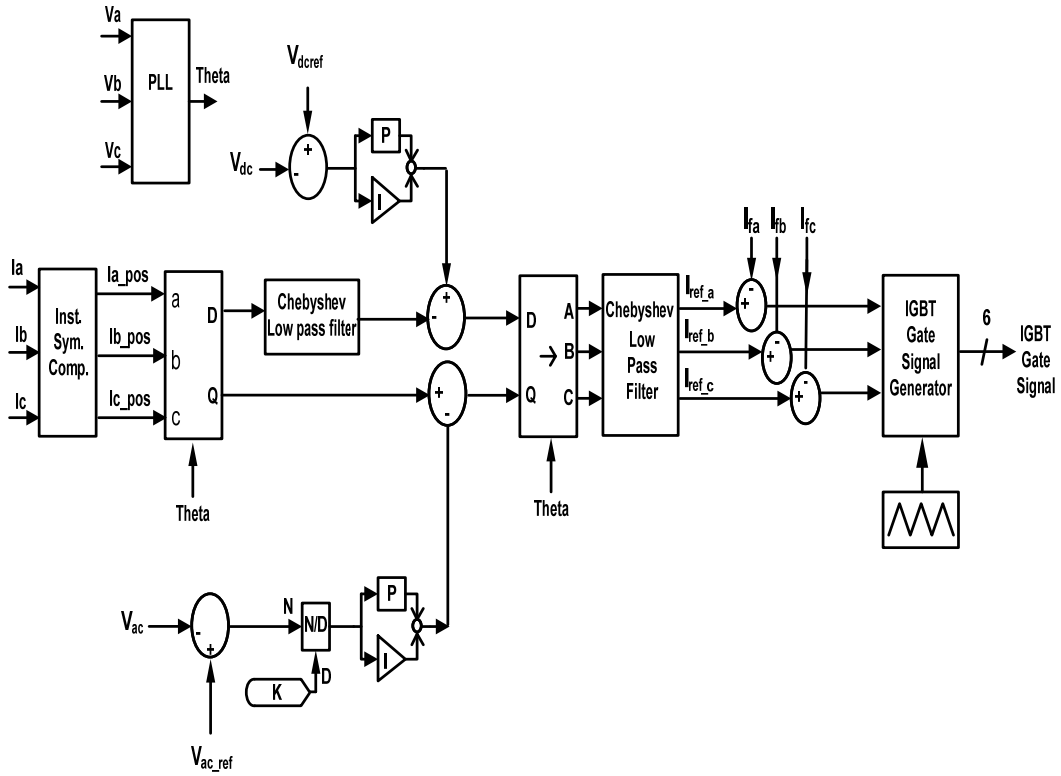


Figure 4.10. Overall control structure of DSTATCOM

5. TEST SYSTEM AND SIMULATION RESULTS

5.1. Test System

The modeled system has been tested with linear and non-linear load on different conditions. System test parameters are listed in Table 5.1 - 5.3.

Table 5.1. PSCAD/EMTDC simulation parameters

PSCAD/EMTDC Parameters	
Solution time step	20 µs
Channel plot step	20 µs
Duration of simulation run	2 s

Table 5.2. System parameters

System Parameters	
Voltage source	400V
Fundamental frequency	50 Hz
Impedance of feeder	R=0.02 Ω, X=0.16 mH
Nonlinear load	A three-phase diode rectifier that supplies a load of $1.15 + j0.0314\Omega$
Linear load	R= 1.3 Ω, X=3.3 mH
DC link voltage	680V
DC link capacitor	60 mF
Switching frequency	10 kHz
LCL filter	L_i=0.07 mH, L_g=0.03 mH, C_f=0.083 mF, R_d=0.8 Ω
Resonance frequency of filter	2.2 kHz

Table 5.3. Control system parameters

DC Link PI Controller Parameters	
Proportional gain	50
Integral time constant	0.5 s
AC Voltage PI Controller Parameters	
Proportional gain	
Integral time constant	

The power circuit diagram of DSTATCOM system on PSCAD/EMTDC used in this thesis are shown in Figure 5.1.

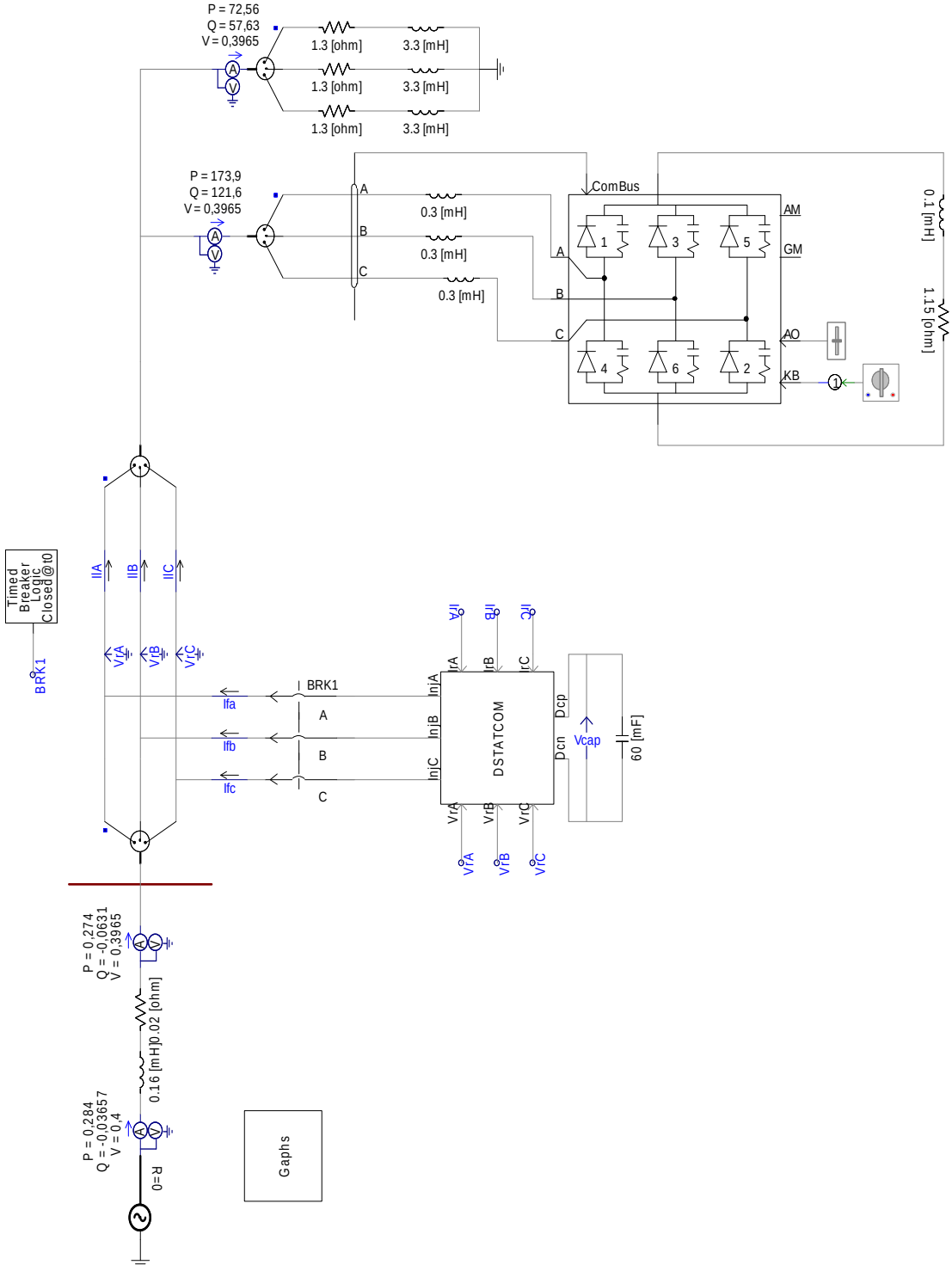


Figure 5.1. PSCAD/EMTDC model of DSTATCOM

5.2. Simulation Results

To show the restoring function of the proposed DSTATCOM and performance of the new control algorithm, the system is tested for the following case studies:

5.2.1. Case 1: Harmonic Mitigation, Voltage Regulation and Reactive Power Compensation

The extraction of harmonic content extracted with Instantaneous Symmetrical Component Theory and Synchronous Reference Frame method. For the reactive power compensation, the fundamental reactive compensation current is calculated for the three phase and the DSTATCOM inject nearly 200kVAr reactive power to network. The DC link voltage is kept constant at 680V. The filtering performances of the system are shown in Figures 5.2 and Figure 5.3.

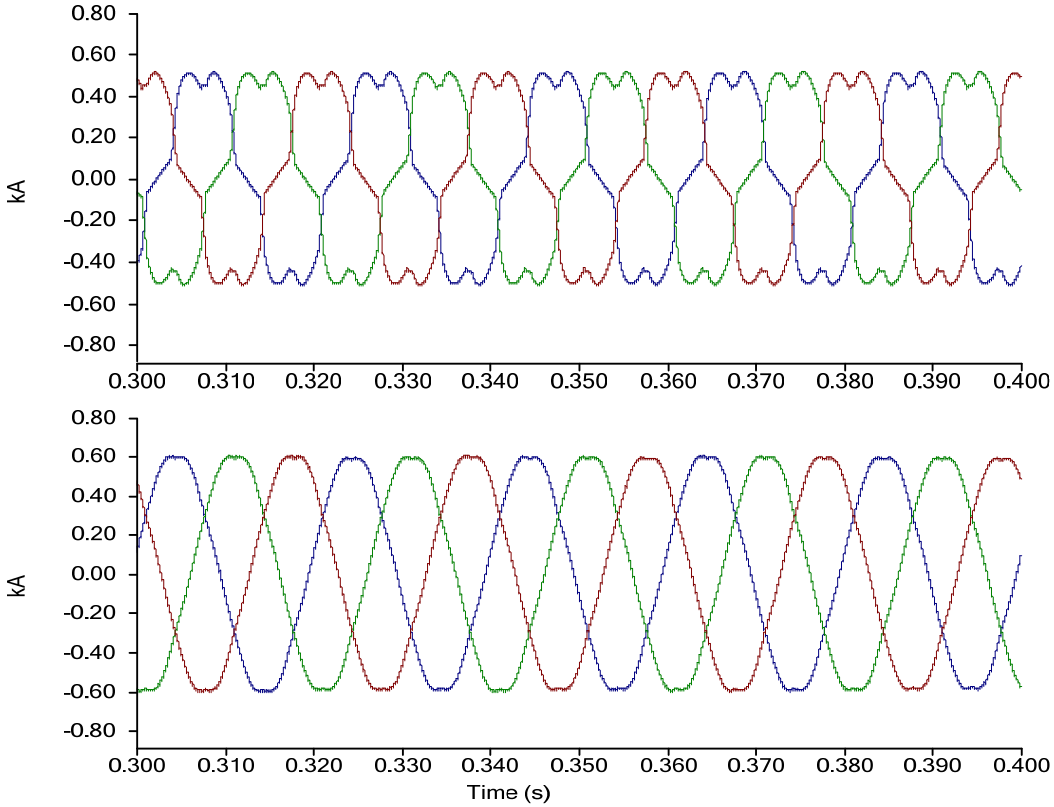


Figure 5.2. PCC current (a) without (b) with DSTATCOM for Case 1

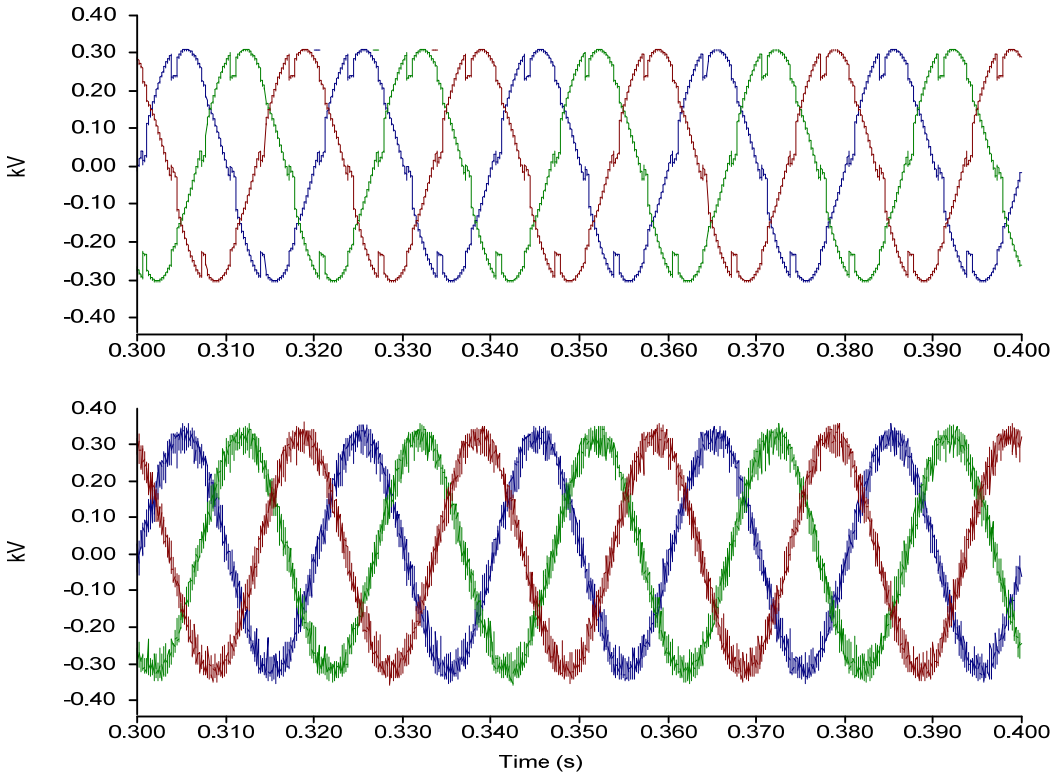


Figure 5.3. PCC voltage (a) without (b) with DSTATCOM for Case 1

The nonlinear/sensitive load current THD is 17.51% before compensation. During fault, load voltage THD is 1.3% and feeder current THD is decreased to 2.2% by VSI. THD values of PCC currents and voltages are shown in Table 5.4.

Table 5.4. THD of harmonics for Case 1

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	17.51	10.0	2.2	1.3
Phase B	17.51	10.0	2.2	1.3
Phase C	17.51	10.0	2.2	1.4

5.2.2. Case 2: Load Balancing, Harmonic Compensation, Reactive Power Compensation and Voltage Regulation

With the simulation of this case, it is clearly shown that the load balance compensation capability. The startup procedure, the extraction of harmonic content are the same as the previous case. For the reactive power compensation, the

fundamental reactive compensation current is calculated for the three phase that is described previous section. The DSTATCOM inject nearly 210kVAr reactive power to network. The DC link voltage is kept constant at 680V. The filtering performances of the system are shown in Figure 5.4 and Figure 5.5.

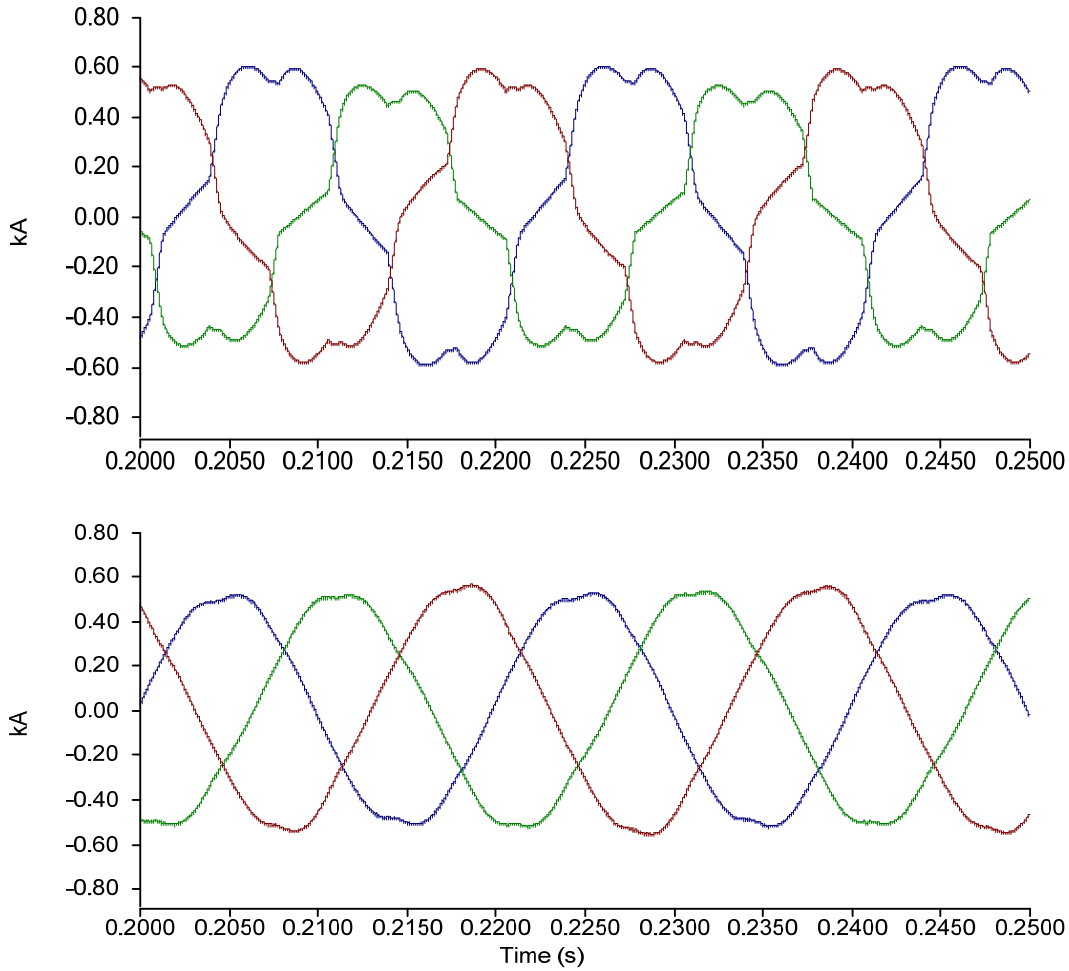


Figure 5.4. PCC current (a) without (b) with DSTATCOM for Case 2

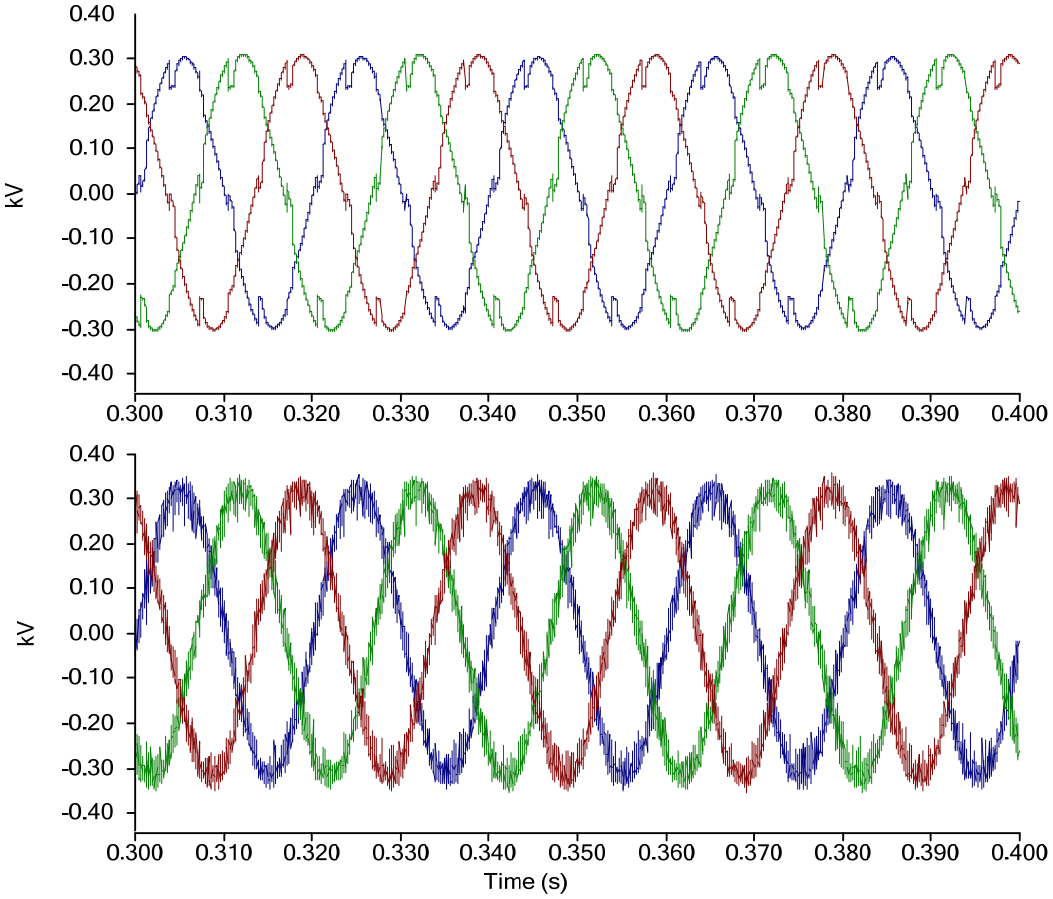


Figure 5.5. PCC voltage (a) without (b) with DSTATCOM for Case 2

The nonlinear/sensitive load current THD is 17.8% before compensation. During fault, load voltage THD is 1.4% and feeder current THD is decreased to 2.5% by VSI. THD values of PCC currents and voltages are shown in Table 5.5.

Table 5.5. THD of harmonics for Case 2

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	14.8	9.5	2.5	1.4
Phase B	17.8	9.8	2.5	1.4
Phase C	14.1	8.6	2.5	1.4

5.2.3. Case 3: Harmonic Compensation, Reactive Power Compensation, Voltage Regulation and Balanced Voltage Sag (15%)

In Case 3, the three-phase balanced fault occurs and 15% voltage sag takes place during the period 0.5-1.5s. The startup procedure, the extraction of harmonic content are the same as the previous case. For the reactive power compensation, the fundamental reactive compensation current is calculated for the three phase that is described previous section. The DSTATCOM injects nearly 320kVAr reactive power to network. DC link capacitor voltage (V_{DC}) level is 680V, even when the voltage sag occurs. The filtering performances of the system are shown in Figures 5.6-5.10.

The three-phase faults are known as the worst-case fault in the system. DSTATCOM performs high performance to inject the more in-phase voltage with proper polarity and phase angle. From the three-phase voltage waveforms, the control strategy of DSTATCOM quickly responses to sudden changes and high quality load voltage waveforms are achieved.

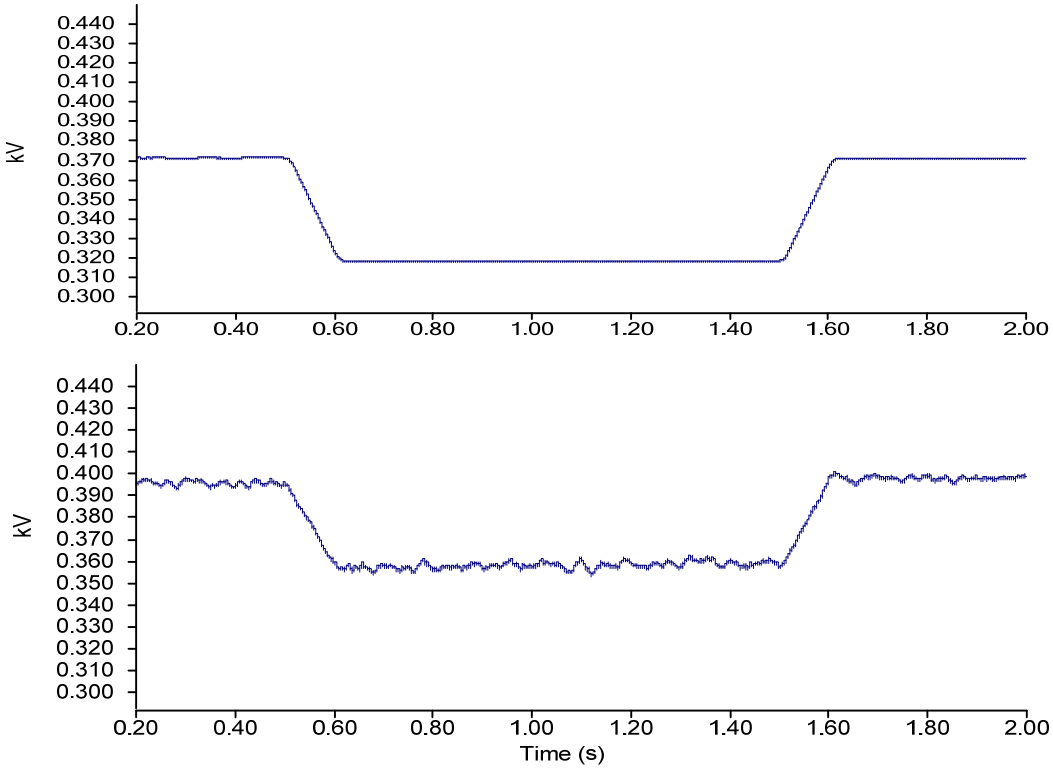


Figure 5.6. RMS voltage of PCC (a) without (b) with DSTATCOM for Case 3

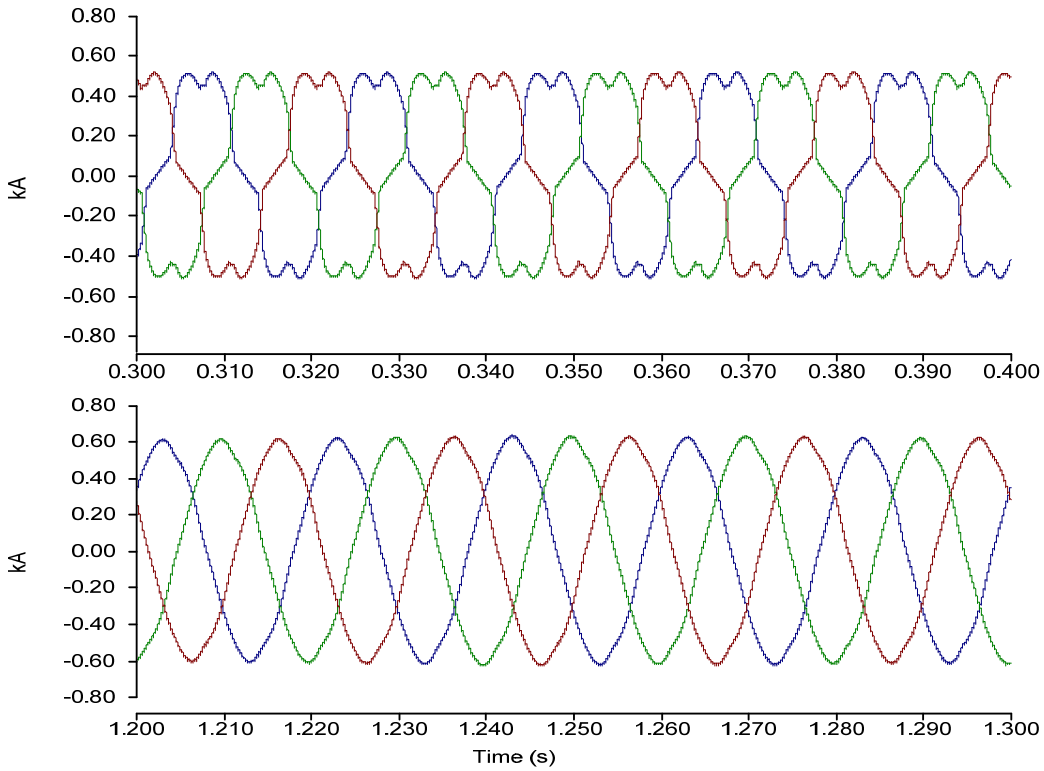


Figure 5.7. PCC current (a) without (b) with DSTATCOM for Case 3

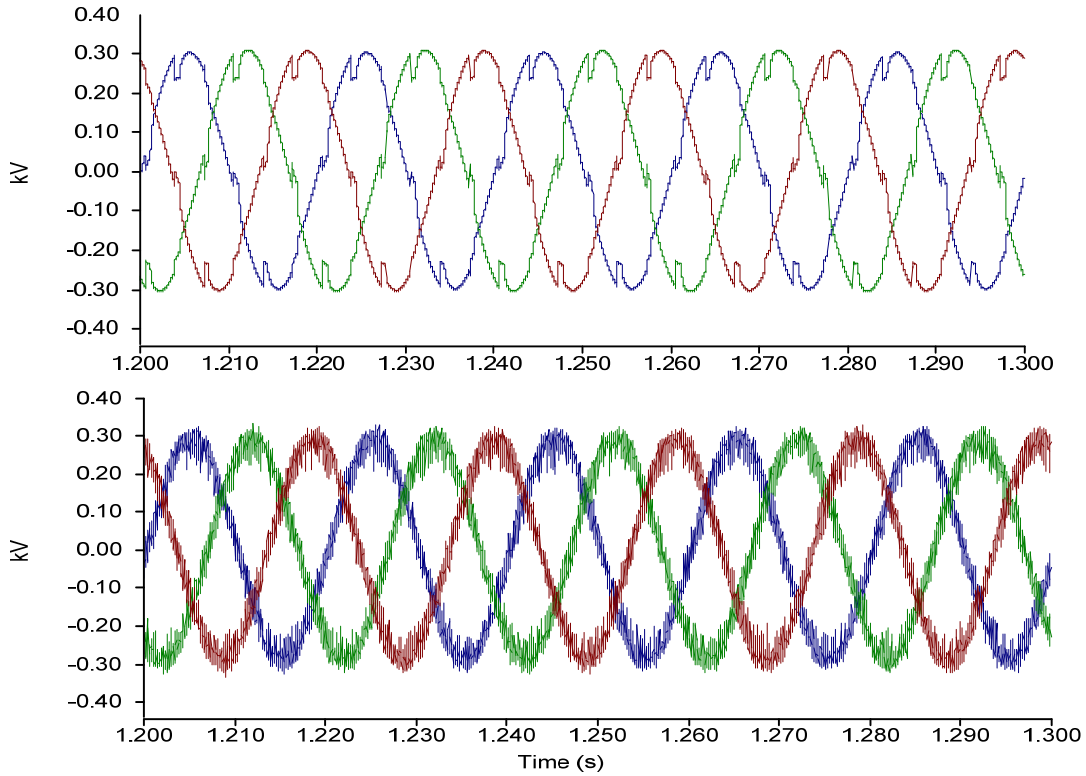


Figure 5.8. PCC voltage (a) without (b) with DSTATCOM for Case 3

The nonlinear/sensitive load current THD is 17.5% before compensation. During fault, load voltage THD is 2.2 % and feeder current THD is decreased to 1.4% by VSI. THD values of PCC currents and voltages are shown in Table 5.6.

Table 5.6. THD of harmonics for Case 3

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	17.5	10.0	2.2	1.4
Phase B	17.5	10.0	2.2	1.4
Phase C	17.5	10.0	2.2	1.4

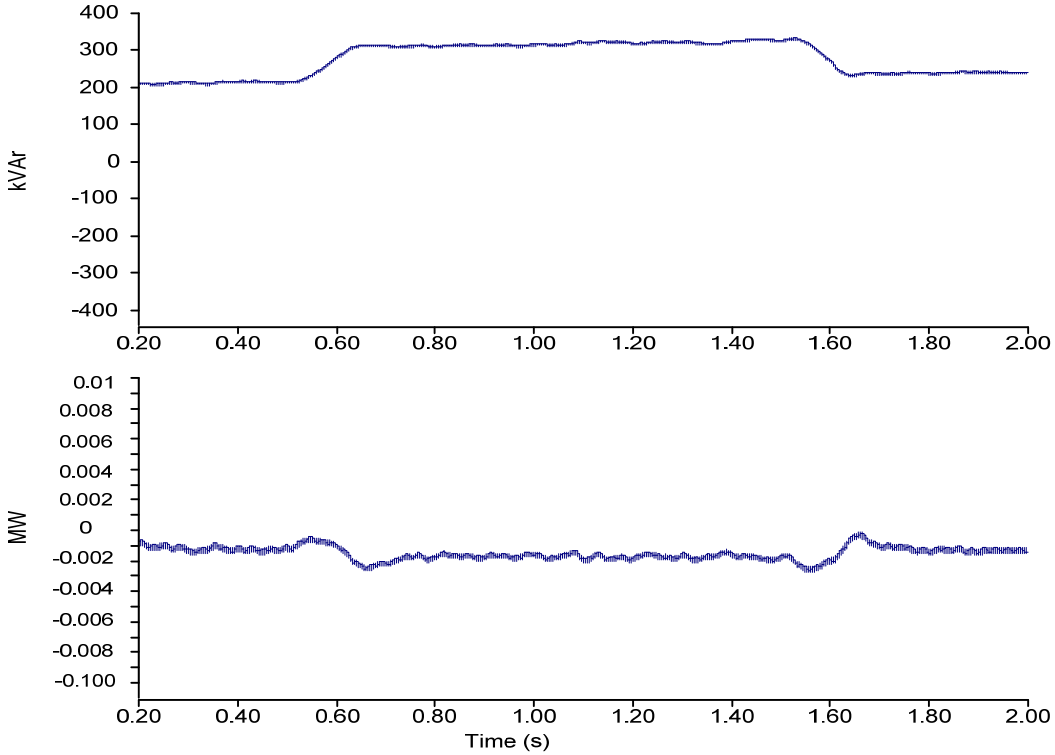


Figure 5.9. Injected reactive power and absorbed active power for Case 3

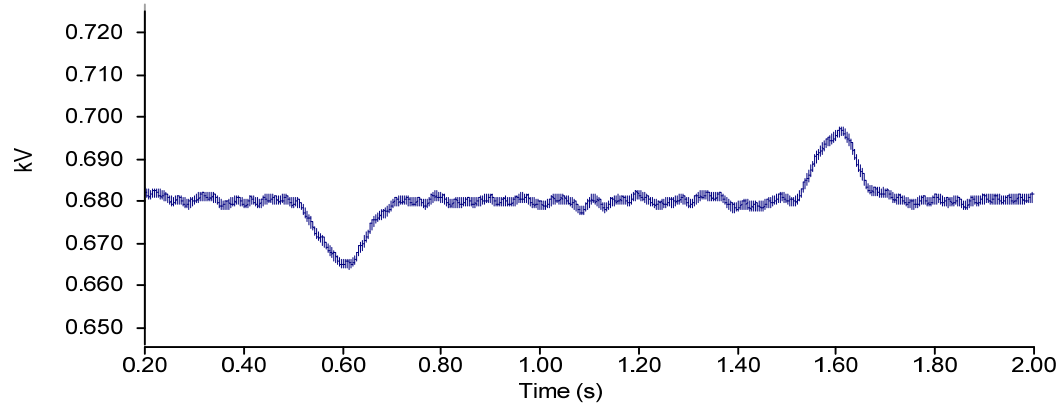


Figure 5.10. DC link voltage for Case 3

5.2.4. Case 4: Load Balancing, Harmonic Compensation, Reactive Power Compensation, Voltage Regulation, Balanced Voltage Sag Mitigation (15%)

In this case, load balancing, harmonic compensation, reactive power compensation, voltage regulation and balanced voltage sag mitigation are simultaneously performed during the period 0.5-1.5s. The startup procedure, the extraction of harmonic content are the same as the previous case. For the reactive power compensation, the fundamental reactive compensation current is calculated for the three phase that is described previous section. The DSTATCOM injects nearly 320 kVAr reactive power to network during the period 0.5-1.5s. DC link capacitor voltage (V_{DC}) level is 680V in this situation. The filtering performances of the system are shown in Figures 5.11-5.15.

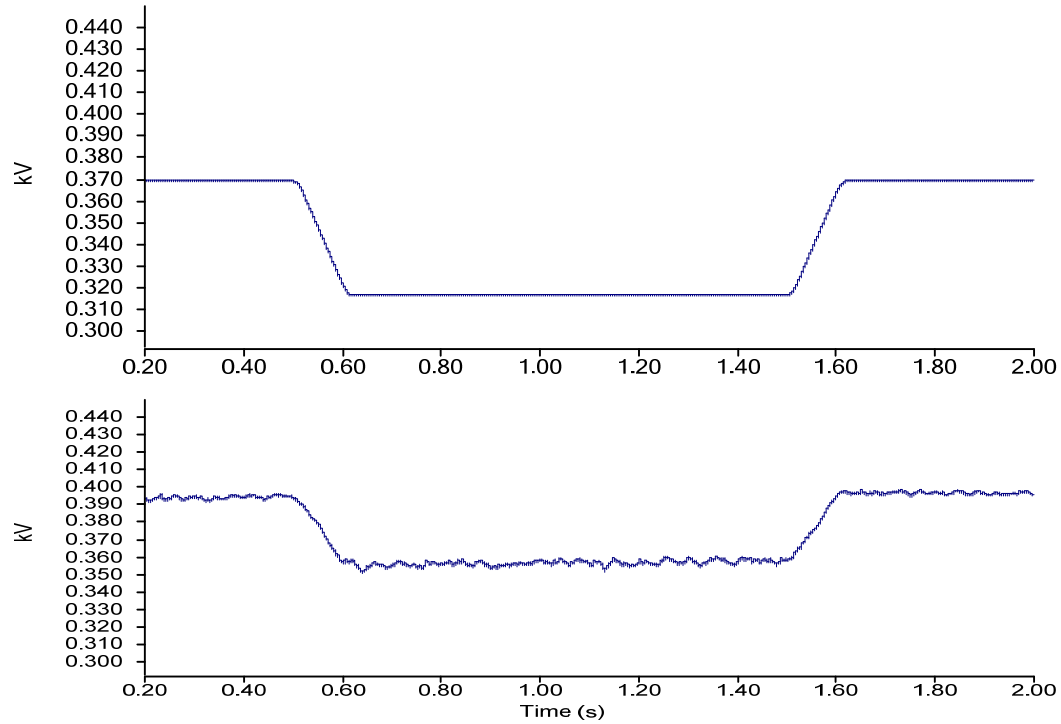


Figure 5.11. RMS voltage of PCC (a) without (b) with DSTATCOM for Case 4

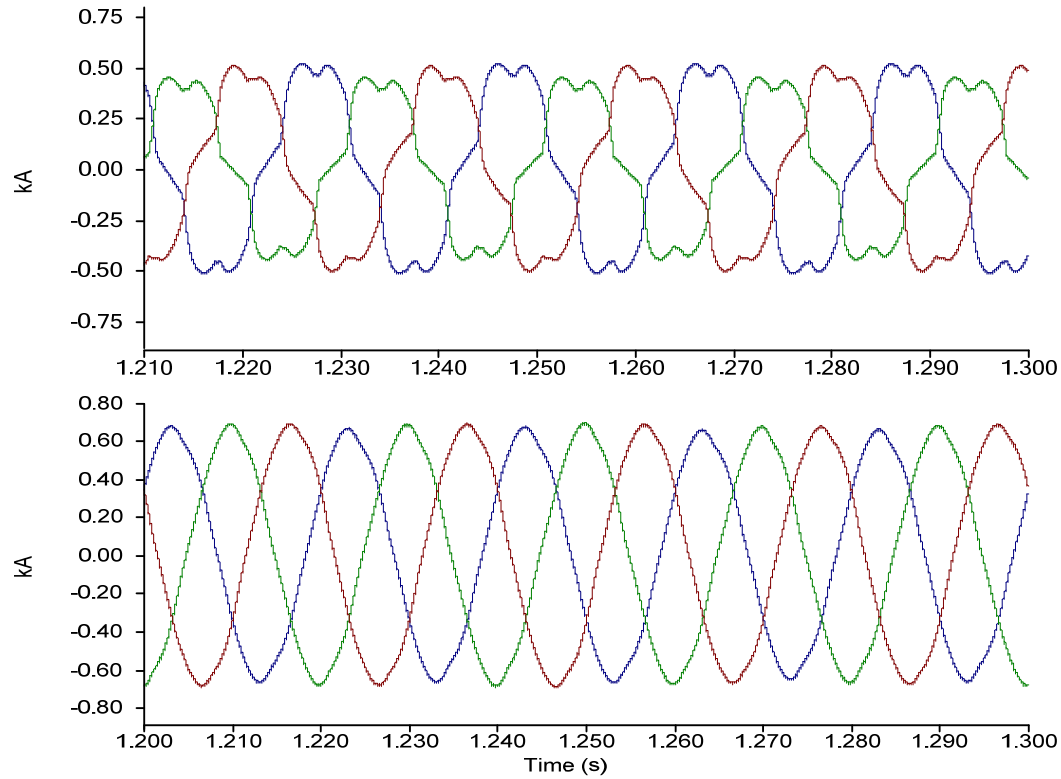


Figure 5.12. PCC current (a) without (b) with DSTATCOM for Case 4

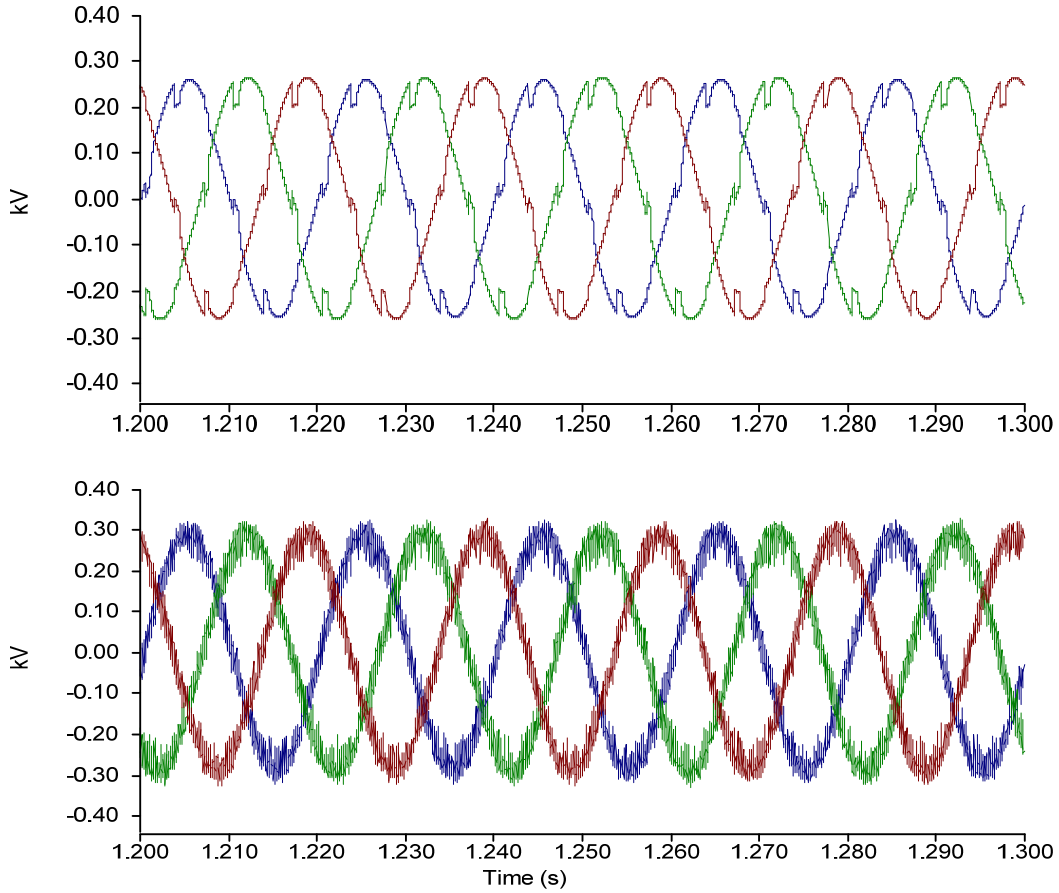


Figure 5.13. PCC voltage (a) without (b) with DSTATCOM for Case 4

The nonlinear/sensitive load THD is 17.8% before compensation. During fault, load voltage THD is 2.4% and feeder current THD is decreased to 1.4% by VSI. THD values of PCC currents and voltages are shown in Table 5.7.

Table 5.7. THD of harmonics for Case 4

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	14.8	9.5	2.4	1.4
Phase B	17.8	9.8	2.4	1.4
Phase C	14.1	8.6	2.4	1.4

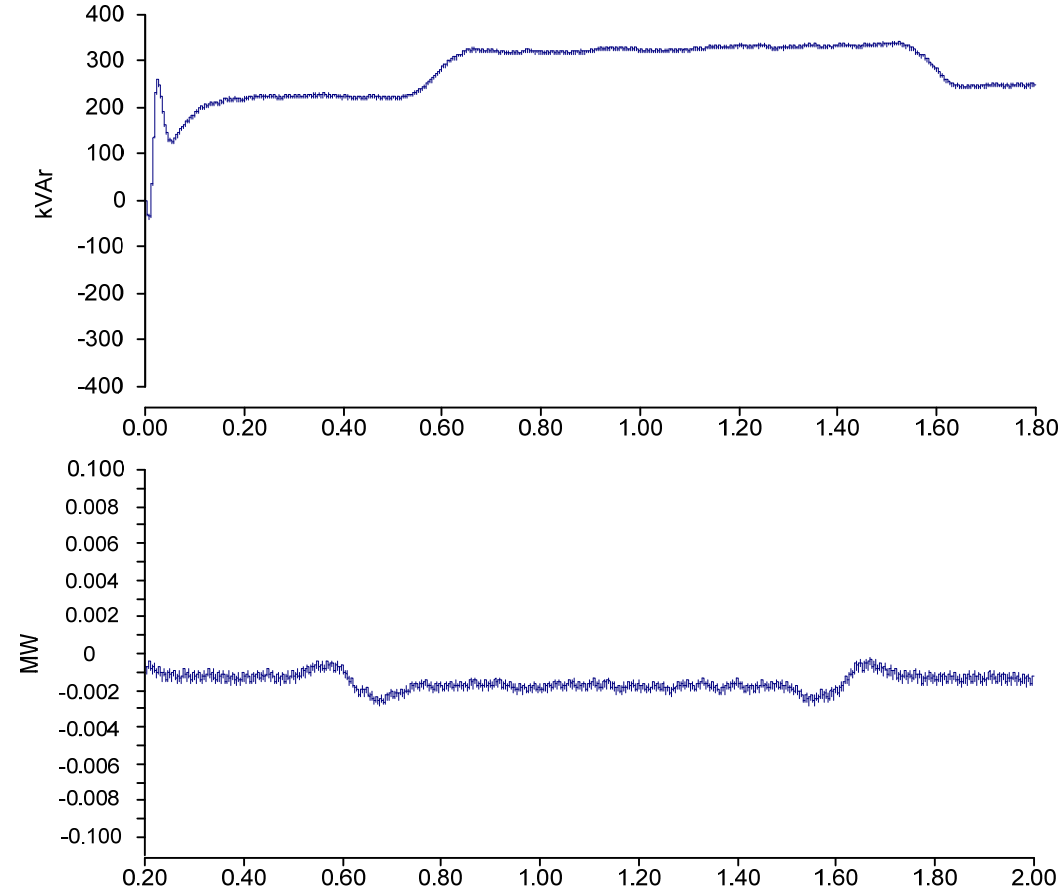


Figure 5.14. Injected reactive power and absorbed active power for Case 4

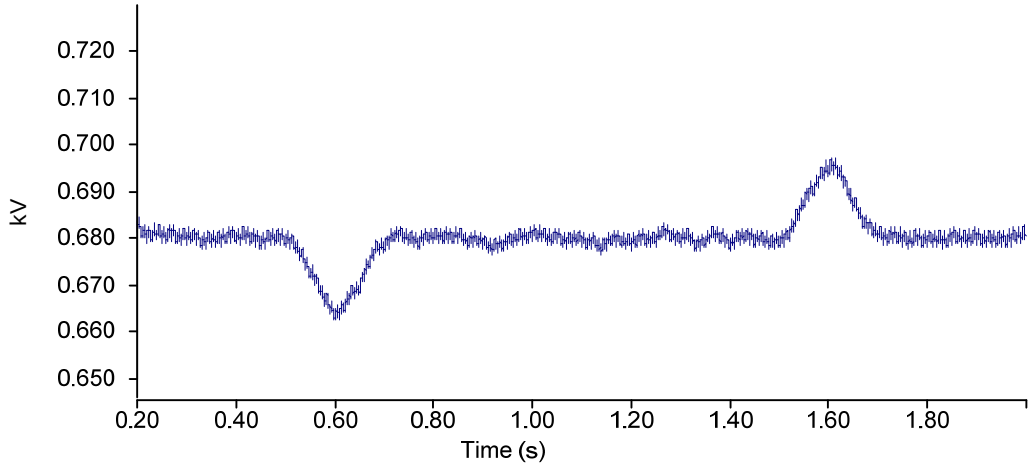


Figure 5.15. DC link voltage for Case 4

5.2.5. Case 5: Harmonic Compensation, Reactive Power Compensation, Voltage Regulation and Balanced Voltage Swell (13%)

VSI of DSTATCOM should be capable of overcoming each phase swell independently and be prepared to mitigate swell on any phase, or any combination of phases. In this case, 13% three phase voltage swell is considered that occurs between 0.5 -1.5 s. RMS trends of PCC, injected and load voltages are shown in Figures 5.16 - 5.20. RMS value of PCC voltage is 420V during voltage swell. DC link capacitor voltage (V_{DC}) is to 680V even when the voltage swell occurs.

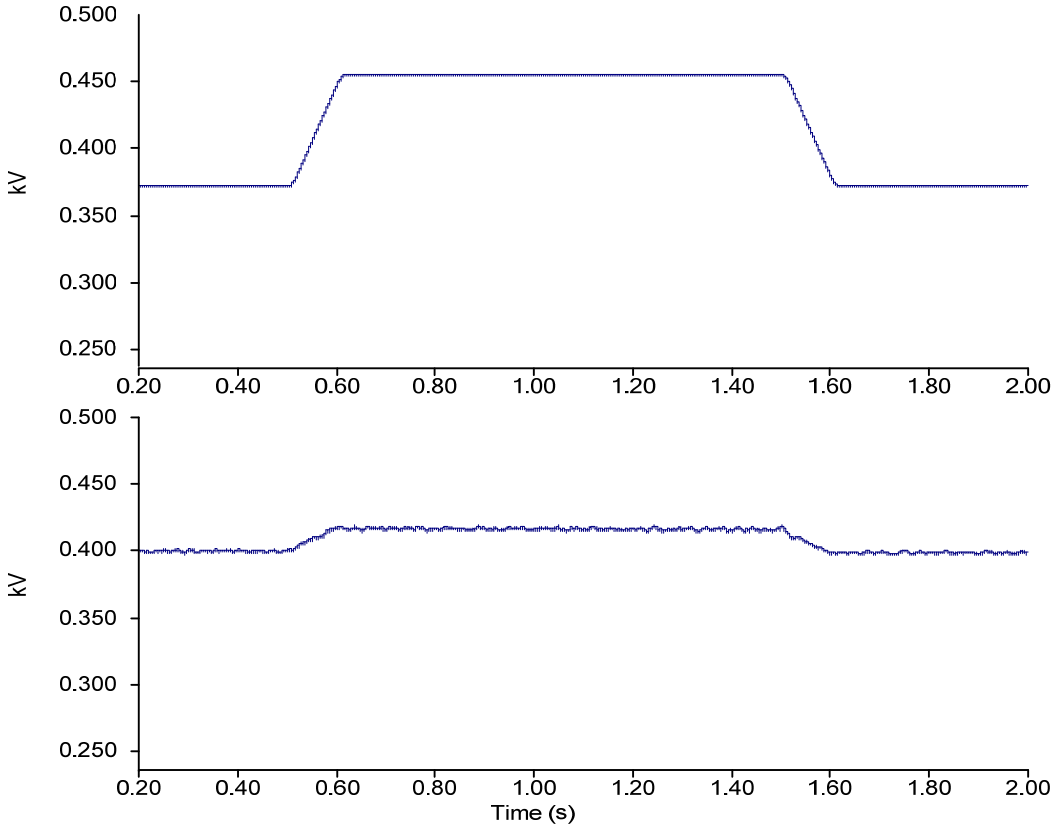


Figure 5.16. RMS voltage of PCC (a) without (b) with DSTATCOM for Case 5

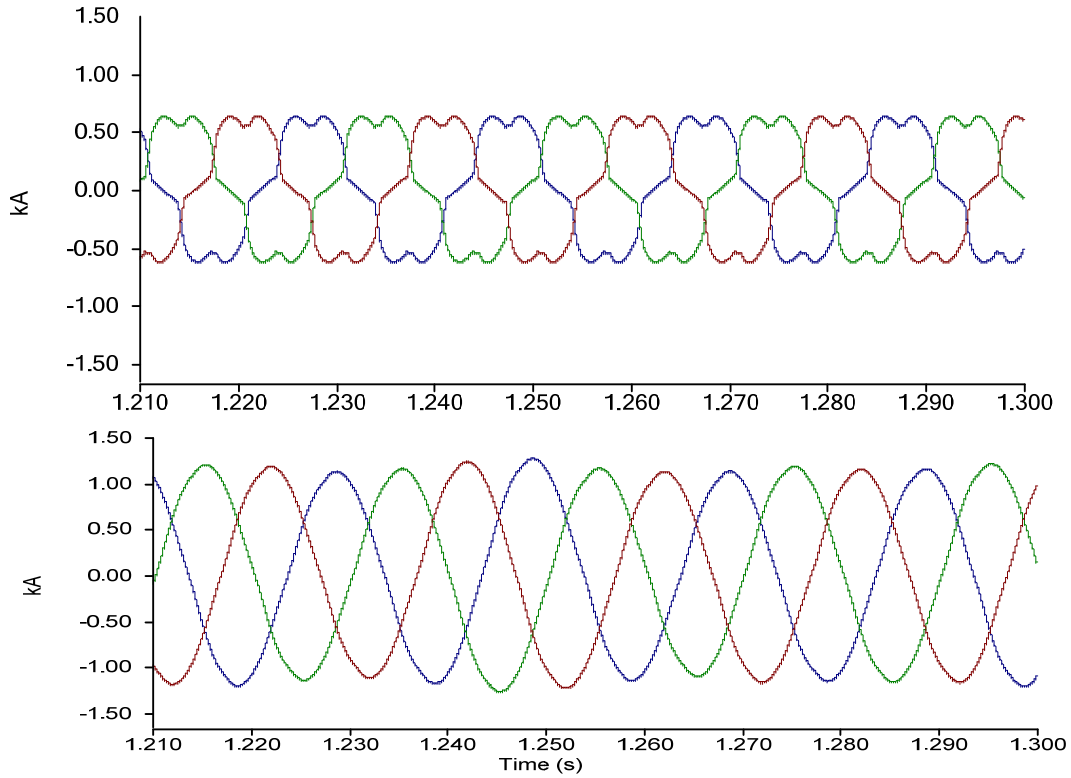


Figure 5.17. PCC current (a) without, (b) with DSTATCOM for Case 5

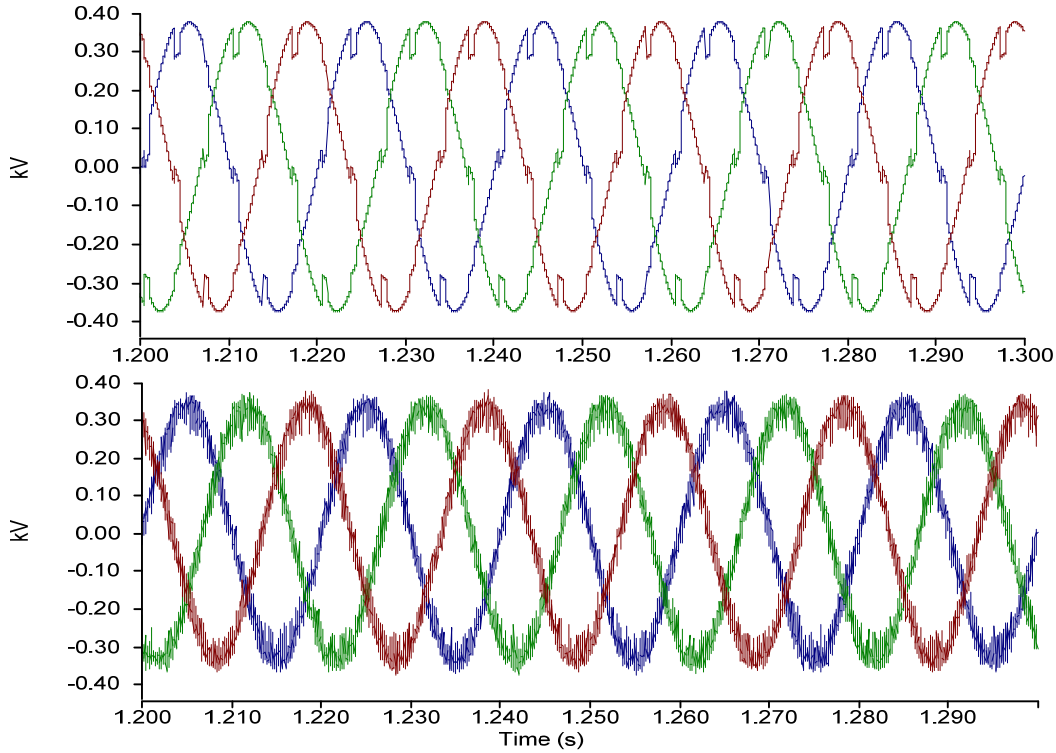


Figure 5.18. PCC voltage (a) without (b) with DSTATCOM for Case 5

THD of the PCC current is always kept below acceptable limits during swell condition by VSI as shown Table 5.8. THD of the load voltage is about 1.45% and THD of the load current is about 1.4% at steady state.

Table 5.8. THD of harmonics for Case 5

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	17.5	9.65	1.4	1.45
Phase B	17.5	9,63	1.2	1.34
Phase C	17.5	9,6	1.3	1.47

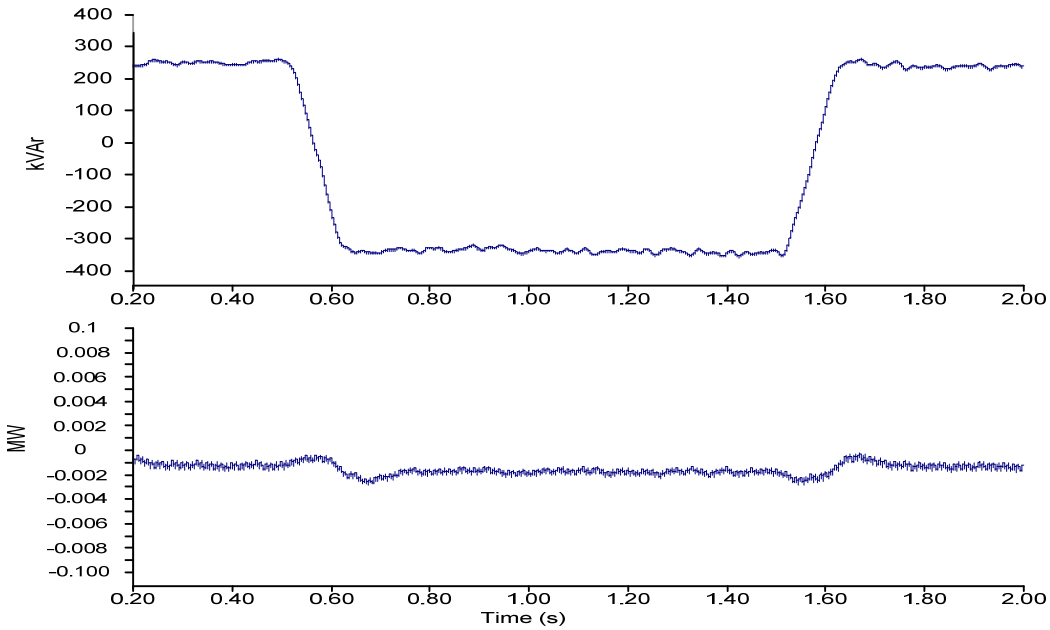


Figure 5.19. Injected reactive power and absorbed active power for Case 5

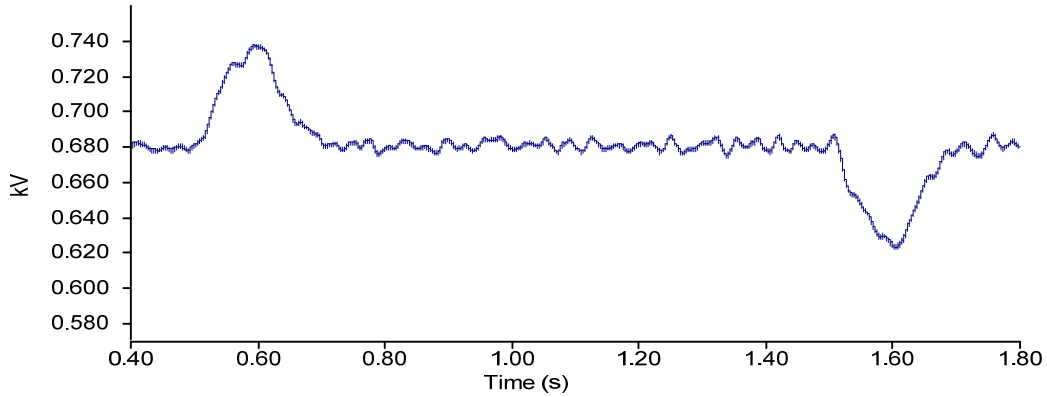


Figure 5.20. DC link voltage for Case 5

5.2.6. Case 6: Load Balancing, Harmonic Compensation, Reactive Power Compensation, Voltage Regulation and Balanced Voltage Swell (13%)

In this Case 6, load balancing, harmonic compensation, reactive power compensation, voltage regulation and balanced voltage swell mitigation are simultaneously performed during the period 0.5-1.5s. The startup procedure, the extraction of harmonic content are the same as the previous cases. For the reactive power compensation, the fundamental reactive compensation current is calculated for the three phase that is described previous sections. The DSTATCOM absorbed nearly 300kVAr reactive power from network during the period 0.5-1.5s. DC link capacitor voltage (V_{DC}) level is 680V in this situation. The filtering performances of the system are shown in Figures 5.21-5.25.

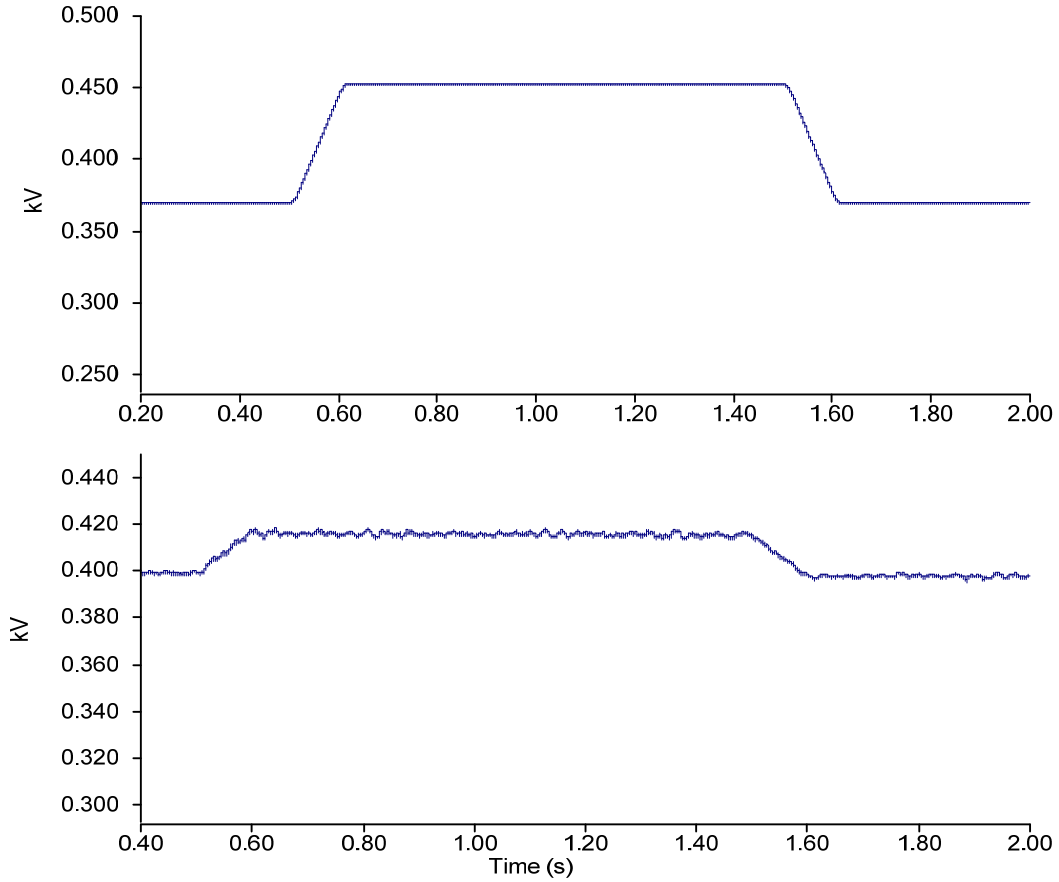


Figure 5.21. RMS voltage of PCC (a) without, (b) with DSTATCOM for Case 6

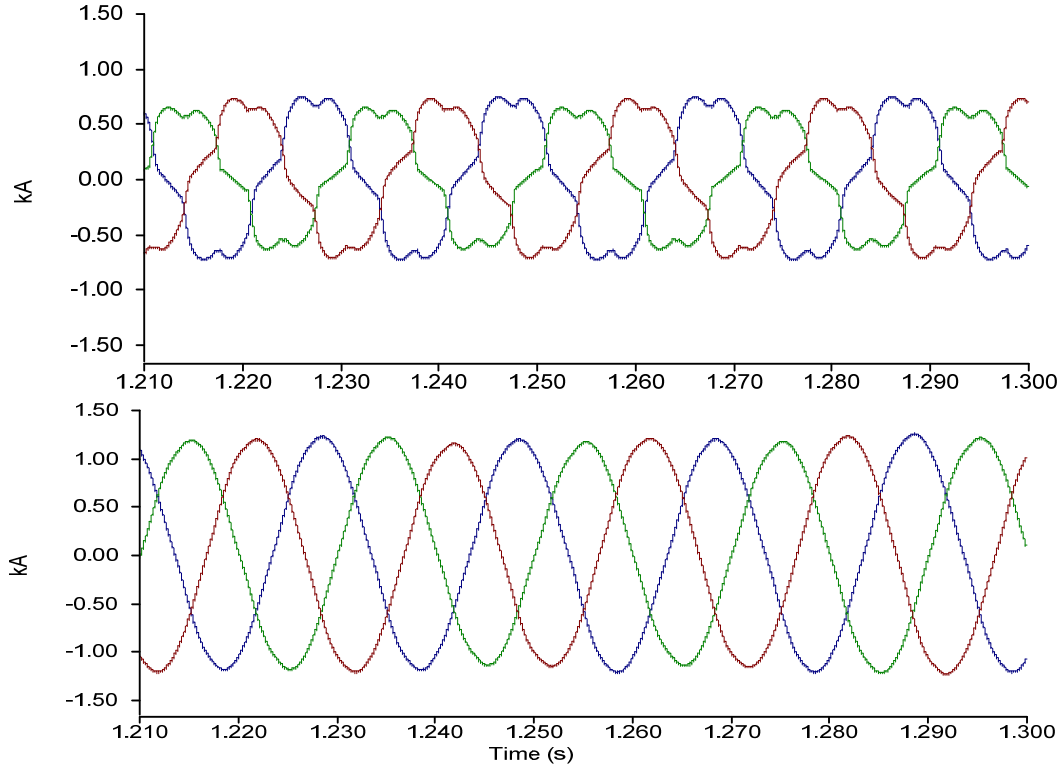


Figure 5.22. PCC current (a) without (b) with DSTATCOM for Case 6

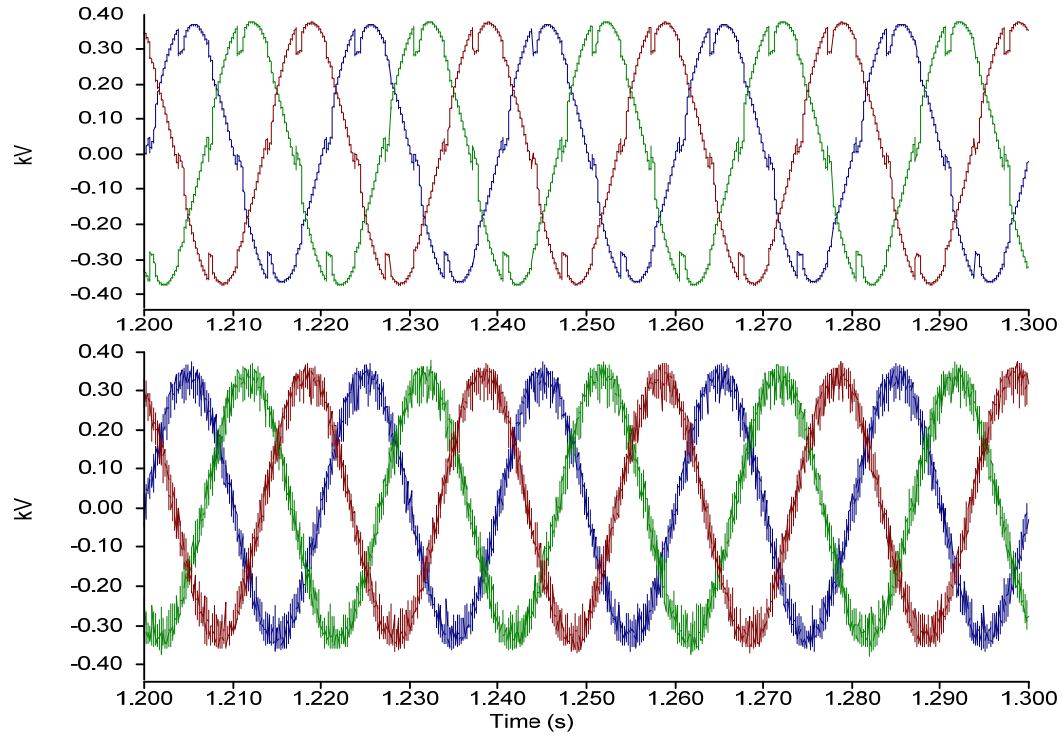


Figure 5.23. PCC voltage (a) without (b) with DSTATCOM for Case 6

THD of the PCC current is always kept below acceptable limits during swell condition by VSI as shown Table 5.9. THD of the load voltage is about 1.45% and THD of the load current is about 1.4% at steady state.

Table 5.9. THD of harmonics for Case 6

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	14.8	9.44	1.7	1.3
Phase B	17.8	9.83	1.7	1.4
Phase C	14.1	8.6	1.5	1.3

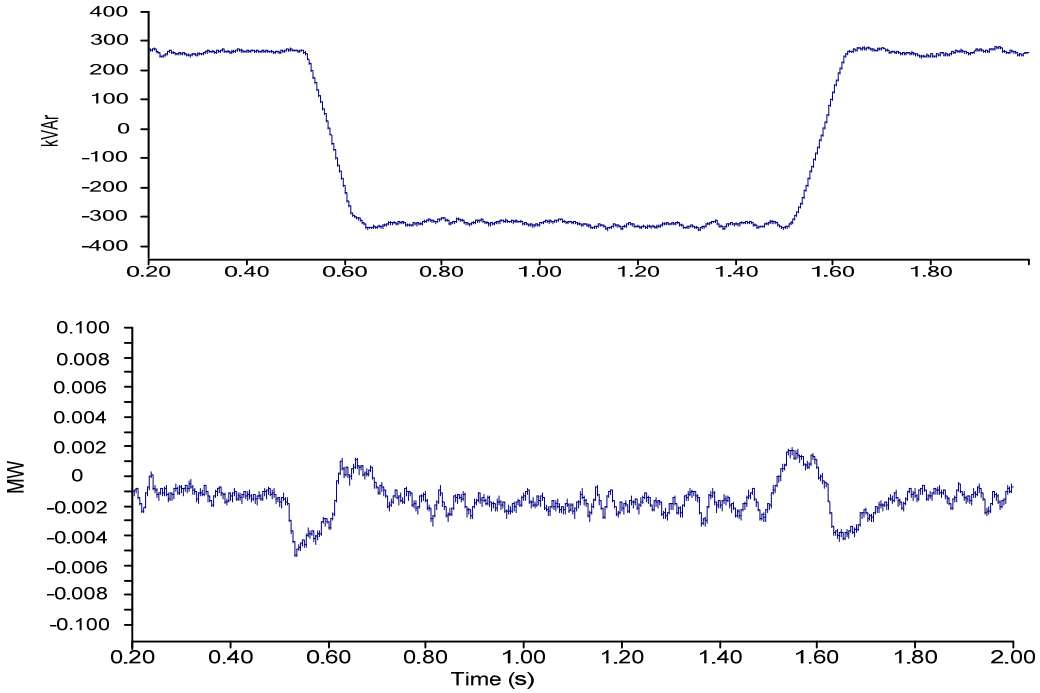


Figure 5.24. Injected reactive power and absorbed active power for Case 6

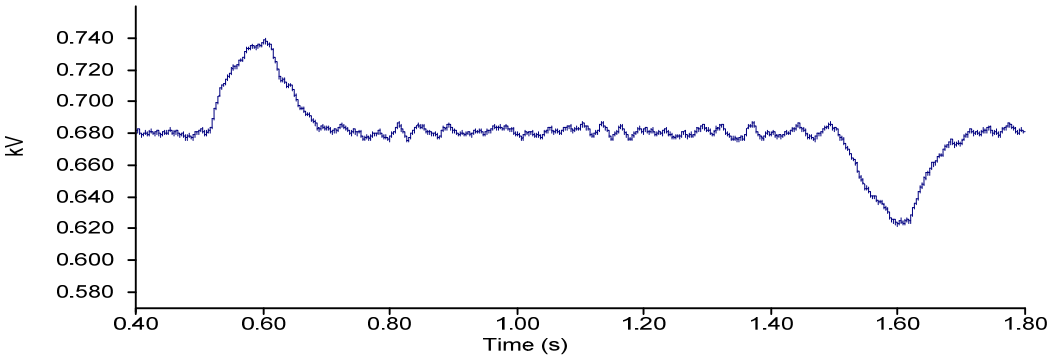


Figure 5.25. DC link voltage for Case 6

5.2.7. Case 7: Harmonic Compensation, Reactive Power Compensation, Voltage Regulation and Unbalanced Voltage Sag (10%)

Most of the faults are single phase line to ground faults (SLGF). The SLGF occurs on phase A resulting in 18% decrease from nominal value during the period 0.5-0.15s. DC link capacitor voltage (V_{DC}) level is 680V in this situation. The filtering performances of the system are shown in Figures 5.26-5.30.

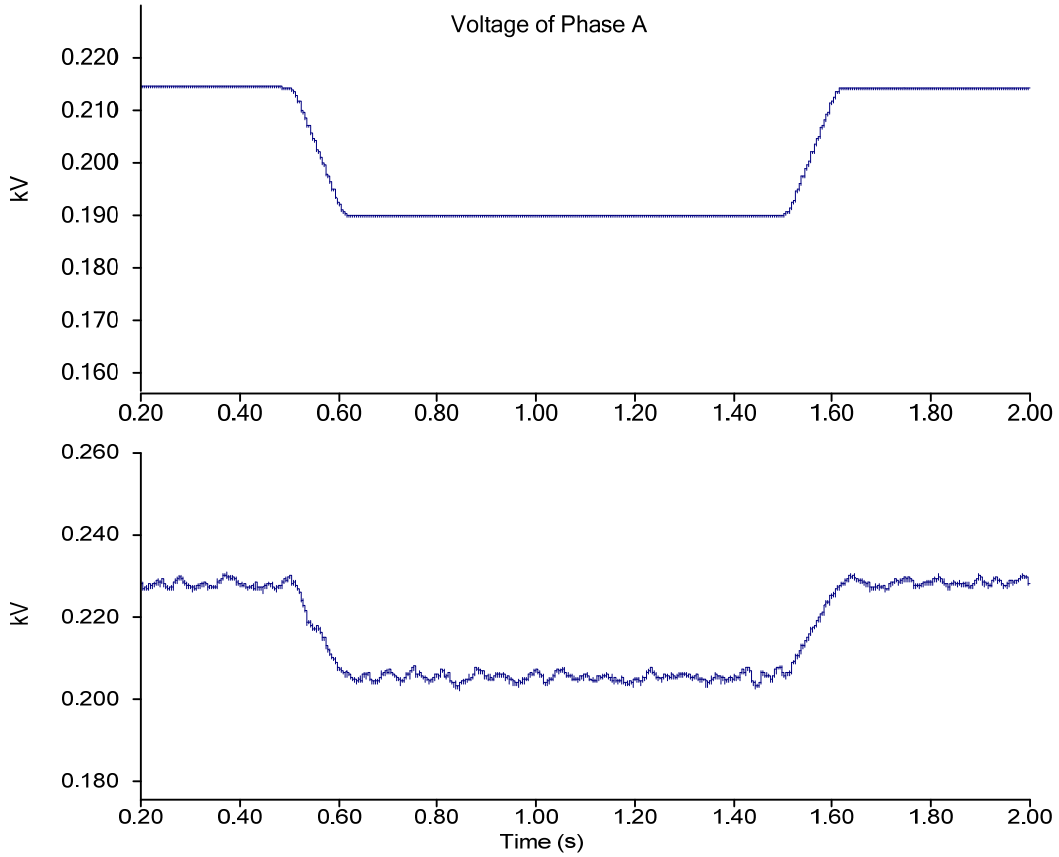


Figure 5.26. RMS voltage of Phase A (a) without (b) with DSTATCOM for Case 7

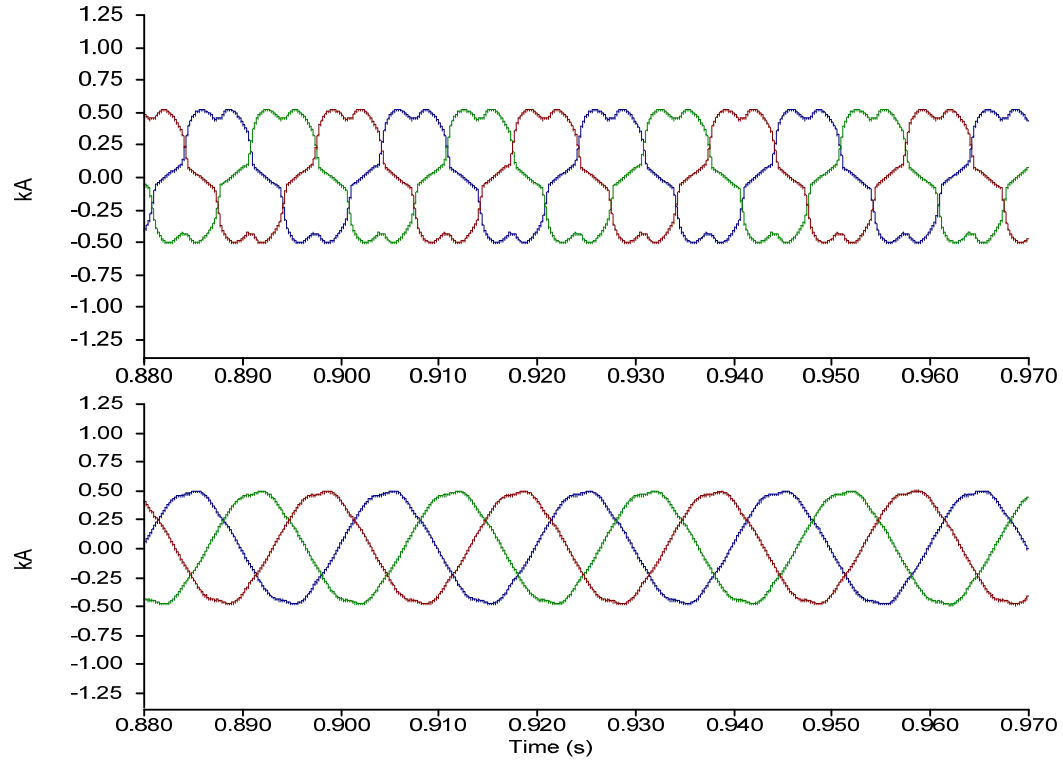


Figure 5.27. PCC current (a) without, (b) with DSTATCOM for Case 7

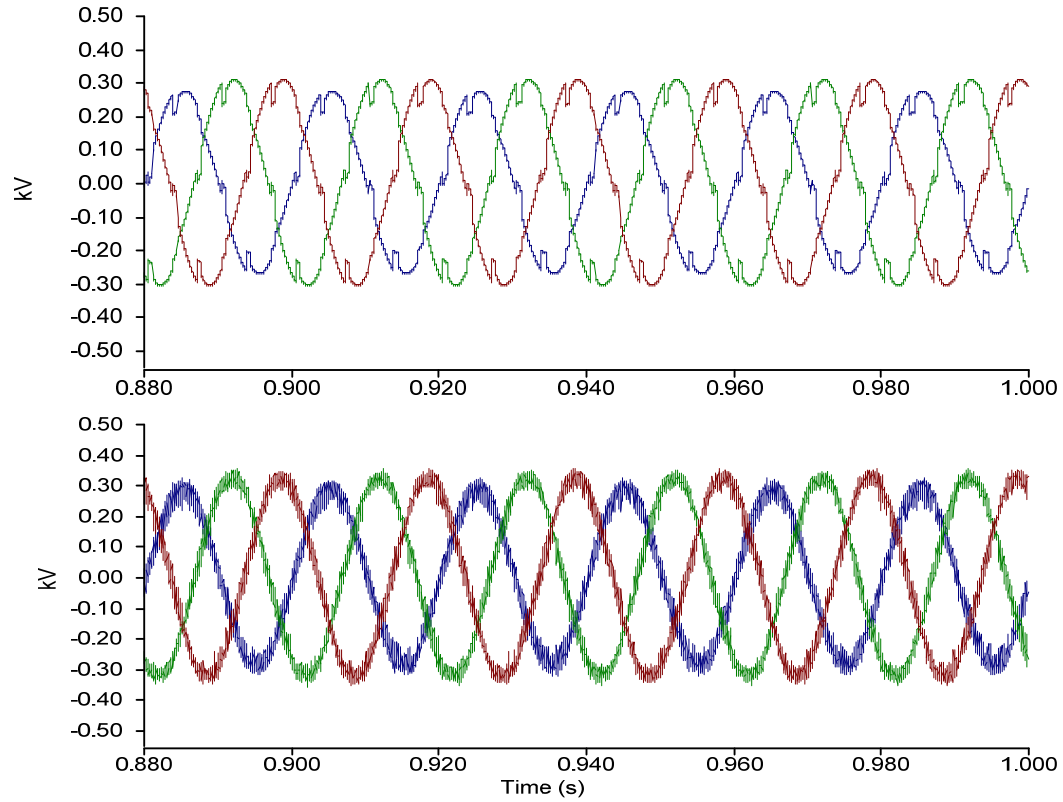


Figure 5.28. PCC voltage (a) without, (b) with DSTATCOM for Case 7

THD of the PCC current is always kept below acceptable limits during swell condition by VSI as shown Table 5.10. THD of the load voltage is about 1.45% and THD of the load current is about 1.4% at steady state.

Table 5.10. THD of harmonics for Case 7

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	18.4	10.4	2.9	1.41
Phase B	17.3	9.3	3.1	1.38
Phase C	16.9	9.3	3.1	1.38

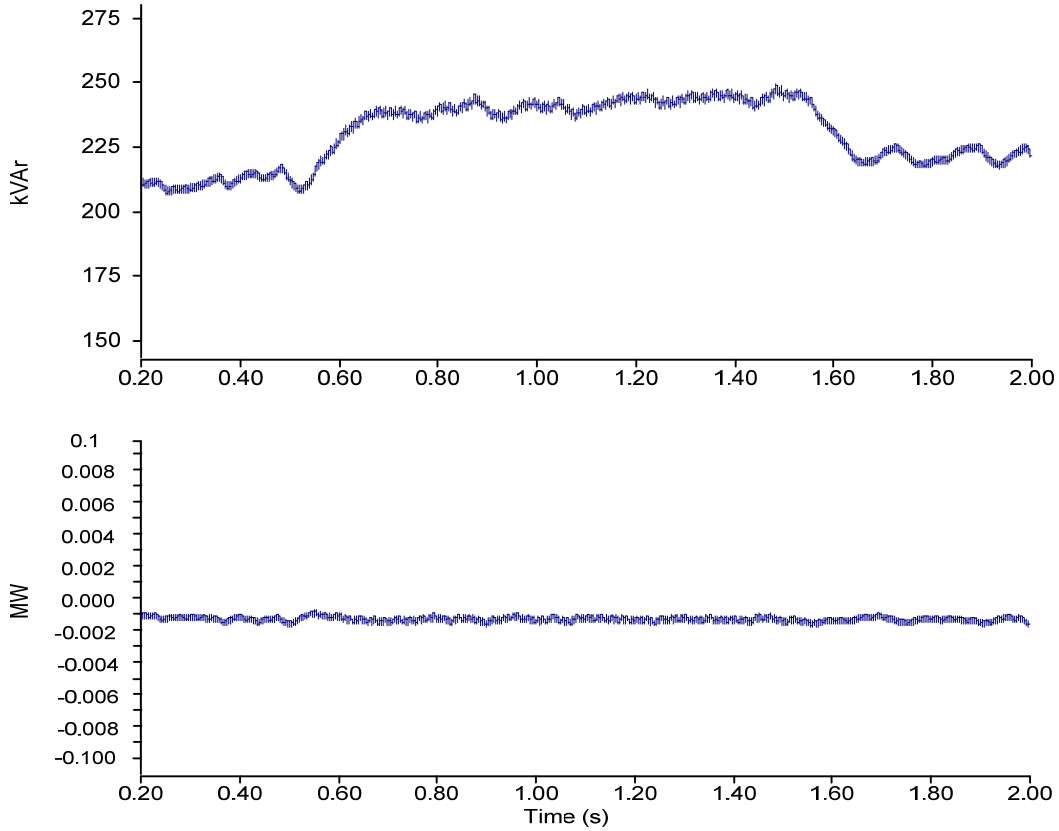


Figure 5.29. Injected reactive power and absorbed active power for Case 7

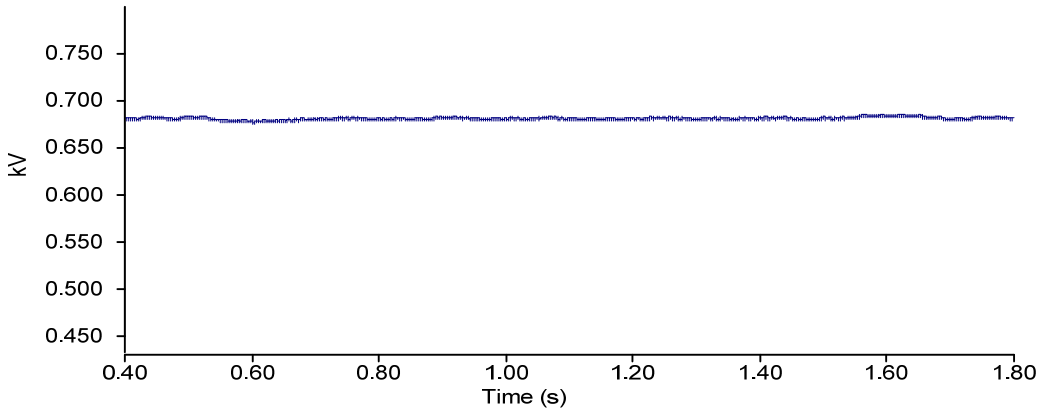


Figure 5.30. DC link voltage for Case 7

5.2.8. Case 8: Load Balancing, Harmonic Compensation, Reactive Power Compensation, Voltage Regulation and Unbalanced Voltage Sag (10%)

Load balancing, harmonic compensation, reactive power compensation, voltage regulation and unbalanced voltage sag mitigation are simultaneously performed during the period 0.5-1.5s. The filtering performances of the system are shown in Figures 5.31-5.35.

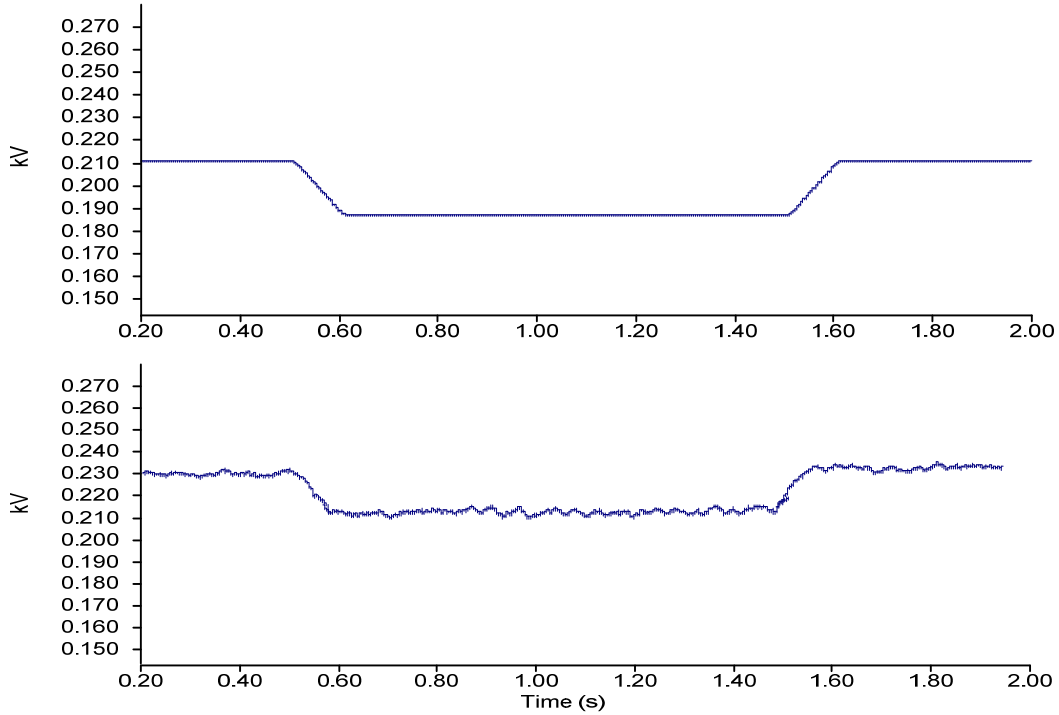


Figure 5.31. RMS voltage of PCC (a) without, (b) with DSTATCOM for Case 8

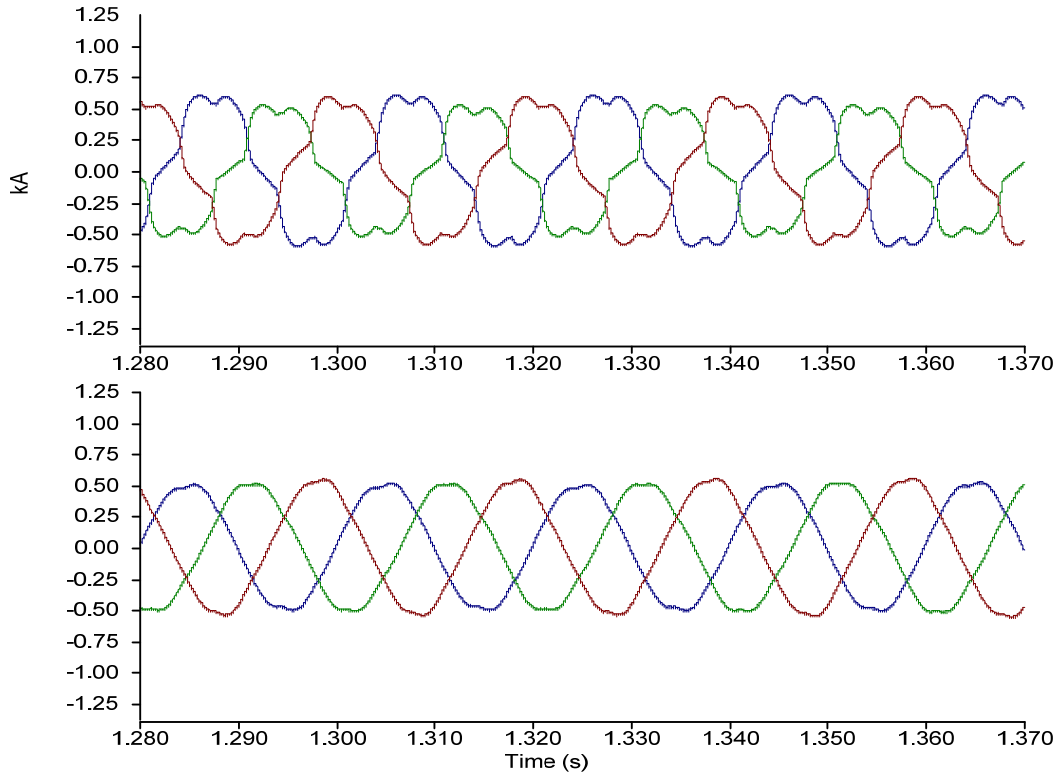


Figure 5.32. PCC current (a) without (b) with DSTATCOM for Case 8

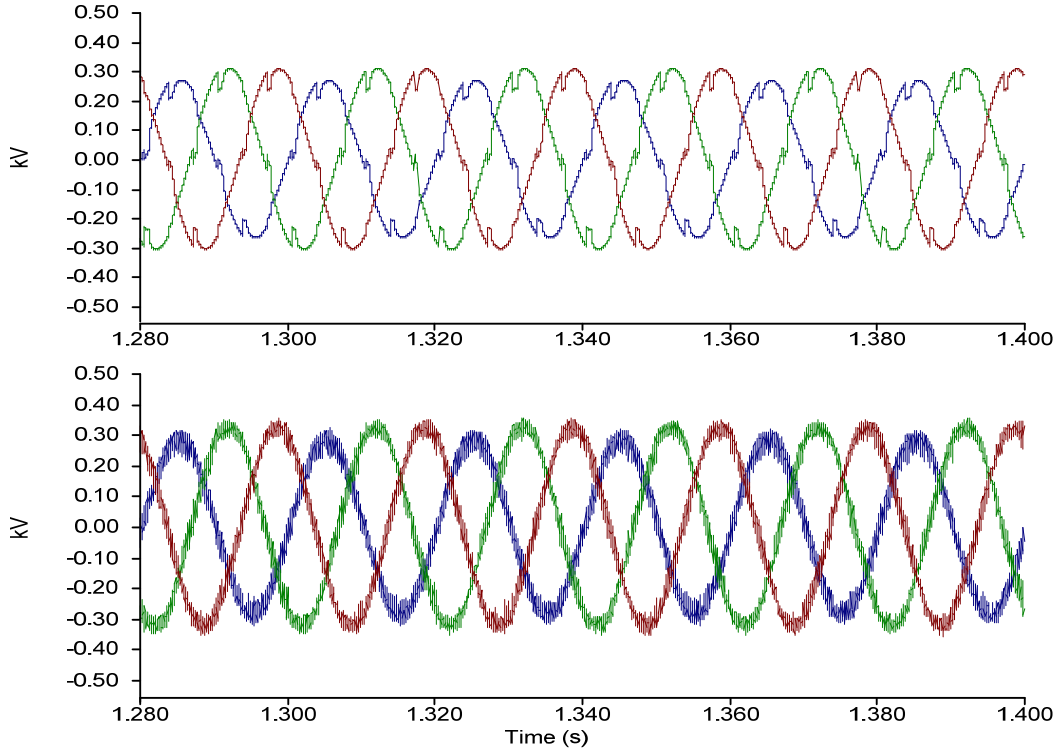


Figure 5.33. PCC voltage (a) without, (b) with DSTATCOM for Case 8

Table 5.11. THD of harmonics for Case 8

Parameter	THD (without DSTATCOM)		THD (with DSTATCOM)	
	Current	Voltage	Current	Voltage
Phase A	18.4	10.4	2.9	1.41
Phase B	17.3	9.3	3.1	1.38
Phase C	16.9	9.3	3.1	1.38

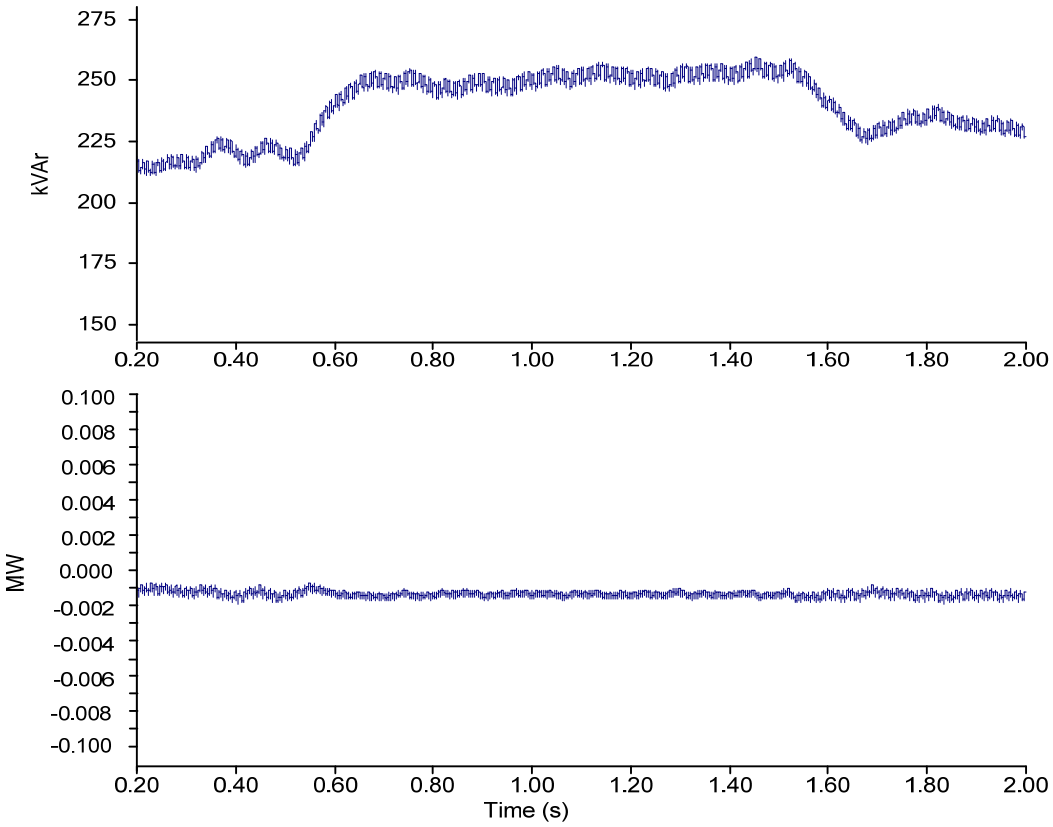


Figure 5.34. Injected reactive power and absorbed active power for Case 8

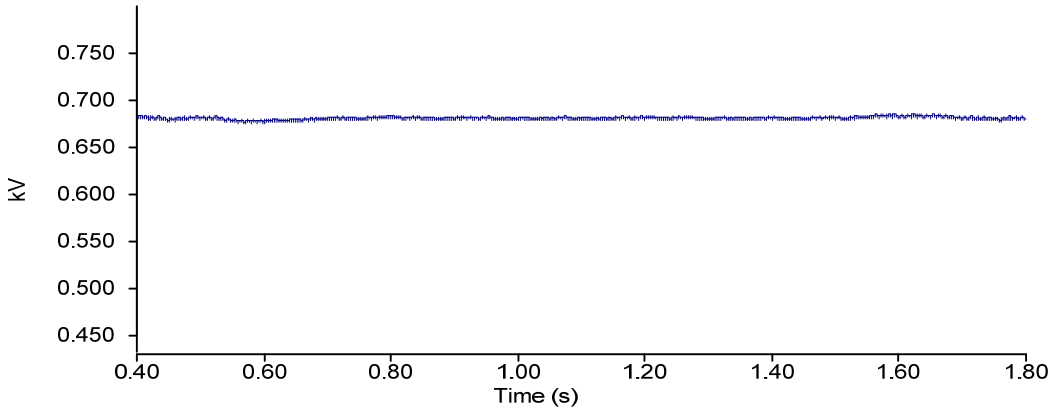


Figure 5.35. DC link voltage for Case 8

6. CONCLUSIONS, CHALLENGES AND FUTURE WORKS

In this thesis, a fast and effective DSTATCOM is proposed for reactive power compensation, voltage regulation, harmonic elimination, balanced voltage sag/swell and unbalanced voltage sag mitigation. The comprehensive literature research was reviewed to understand and design the proposed DSTATCOM. The power quality problems were defined and the main components and operation principle of DSTATCOM were explained in Chapters 1 to 3. In Chapter 4, the design of the proposed DSTATCOM was clarified in detail. The proposed control strategy was composed to generate the reference signal for the system. The performance and efficiency of the proposed system are tested with different simulation cases by PSCAD/EMTDC program in Chapter 5. The analyzed results accomplish that the proposed DSTATCOM performs the harmonic filtering, the reactive power compensation, voltage regulation, balanced voltage sag/swell and unbalanced voltage sag mitigation simultaneously.

- The dq theory based on Instantaneous Symmetrical Component theory is used to generate the reference current from the distorted load current.
- The control strategy does not require a complex computer algorithm. The elimination of transformations, multiplications and divisions makes the control system simple and more reliable. The controller has obtained high performance with relatively low sampling time and switching frequency.
- Instantaneous Symmetrical Component theory is used to obtain balanced reference current under unbalance conditions.
- In dq theory based on Instantaneous Symmetrical Component control strategy, dc voltage controller is used to maintain maintains the DC bus voltage constant by absorbing active power from the grid. AC voltage controller is used to control the magnitude of the voltage at PCC by injecting reactive power.

- By connecting a delta connected inductor-capacitor-inductor (LCL) passive filter at inverter output, the high order harmonics generated by the DSTATCOM can be eliminated due to its superior filtering performance.
- LCL filters give advantage in costs and dynamic since smaller inductors are needed to achieve required performance in damping the switching harmonics comparing with L or LC filters.
- The passive damping control was used for LCL filter, passive damping control strategy is simple and can solve the instable problem caused by the resonant peak well, but there is power loss especially in the high power system.
- The THD value of the source current after the compensation is less than 5%, the harmonic limit is imposed by IEEE-519 & IEC-6000-3 standard.
- The voltage sag/swell is quickly compensated whenever the voltage sag/swell is detected and the PCC voltage is quickly kept at its safe operating region.
- Reactive power is always compensated and the power factor is always kept at higher than 0.98.
- The unbalance voltage is corrected from 10% to 5% of nominal using proposed DSTATCOM.
- The load unbalance compensation is achieved and kept around its optimal value.

Distribution Static Compensators are well established in the literature and market. However, some subjects still need further research and analysis. The recommendations for the future works can be summarized as follows:

- The proposed control strategy and designed DSTATCOM can be tested by connecting the DSTATCOM into a real network where the efficiency and accuracy of the proposed system can be better evaluated.
- The proposed system can be adapted to high-power applications.

- The response of resonance frequency of LCL filter can be analyzed according to different function cases.
- The applicability of the active damping methods to proposed system can be examined.

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